black hat ASIA 2018

When Good Turns Evil

Using Intel SGX to Stealthily Steal Bitcoins

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Moritz Lipp
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Outline

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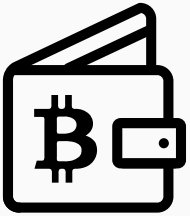

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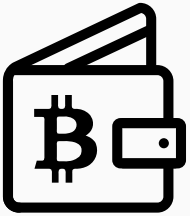

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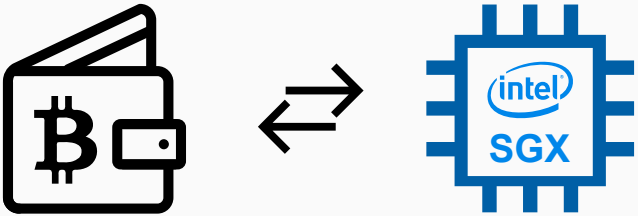

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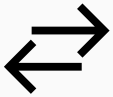

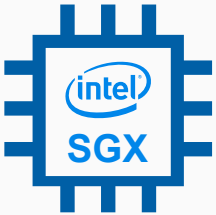

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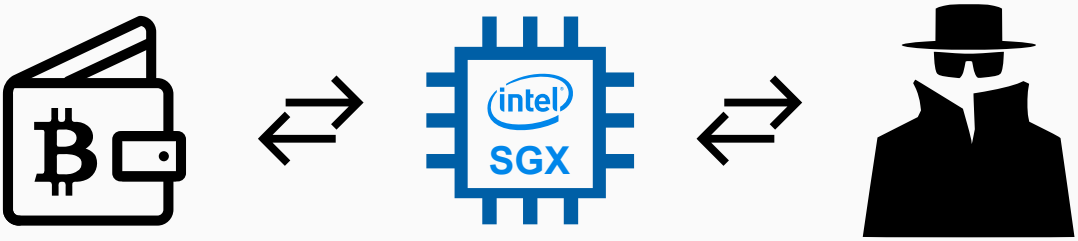

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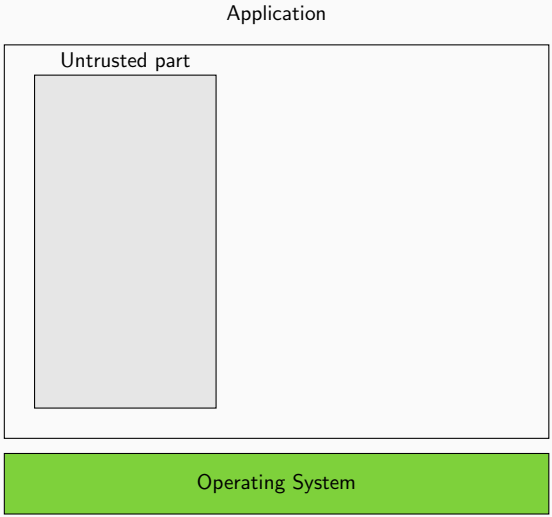
The research team

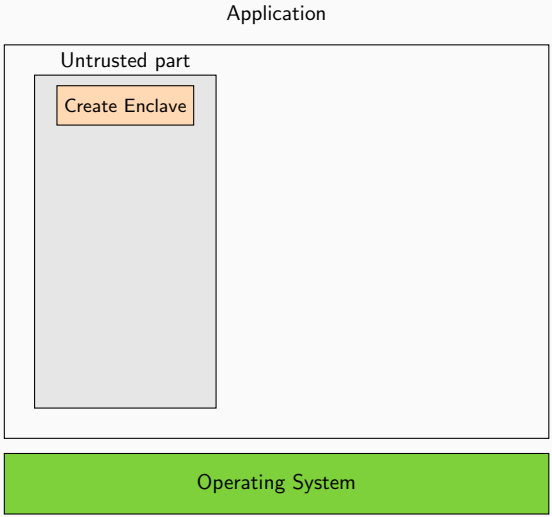
- Daniel Gruss
- Clémentine Maurice
- Samuel Weiser
- Thomas Schuster
- Stefan Mangard

from Graz University of Technology

- Anders Fogh

from G DATA Advanced Analytics


Application
Untrusted part
Operating System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Create Enclave
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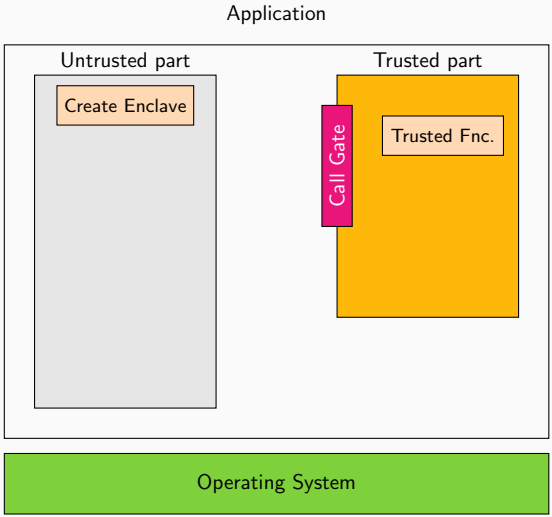
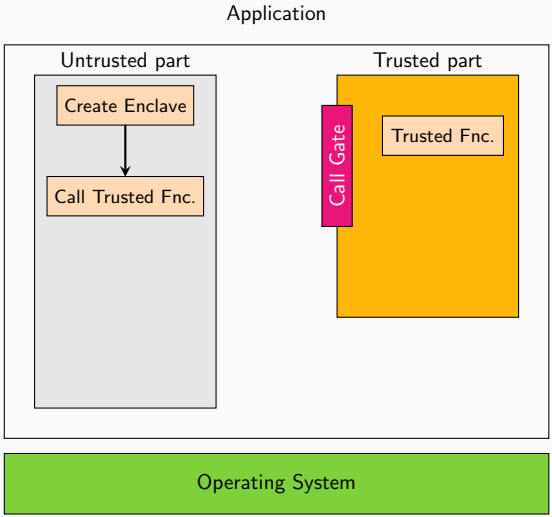

Application
Untrusted part
Create Enclave
Trusted part
Call Gate
Trusted Fnc.
Operating System


Application
Untrusted part
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Call Trusted Fnc.
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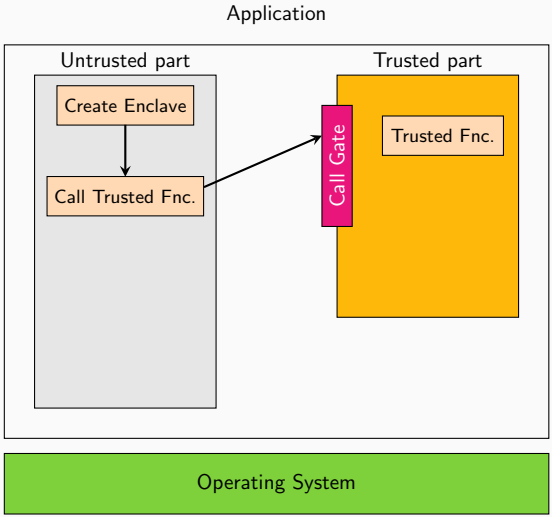
Trusted Fnc.
Operating System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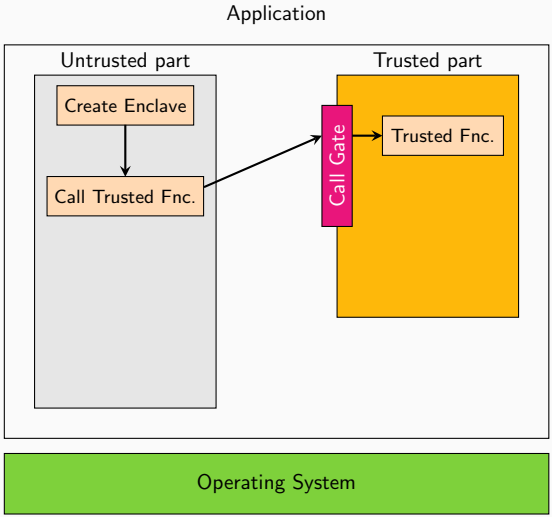
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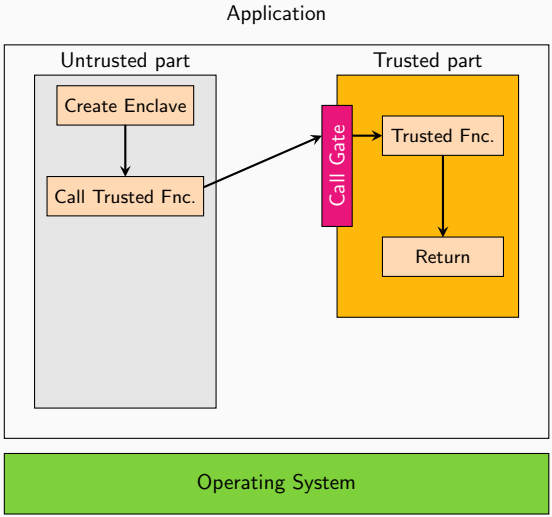
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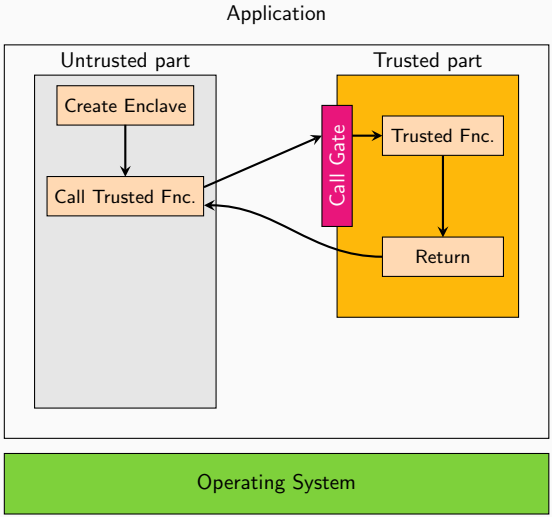
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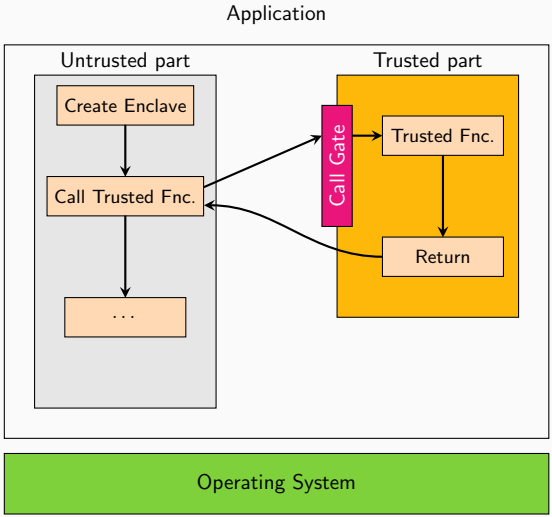
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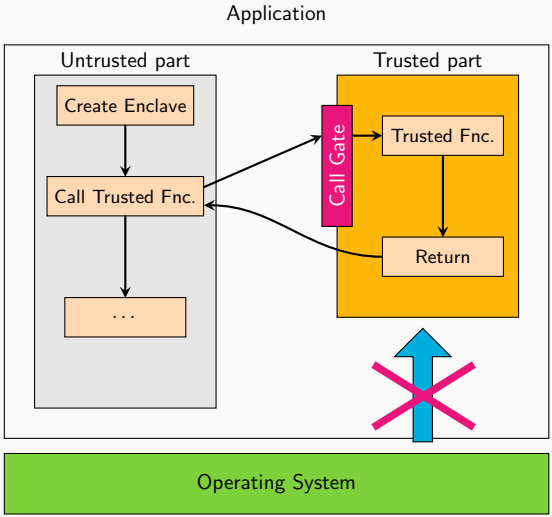
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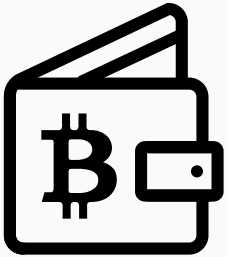
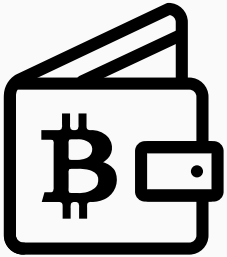


- Ledger SGX Enclave for blockchain applications
- BitPay Copay Bitcoin wallet
- Teechain payment channel using SGX



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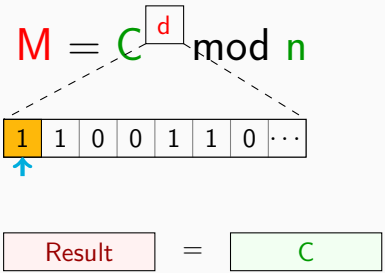
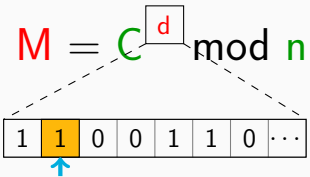
Teechain

[...] We assume the TEE guarantees to hold and do not consider side-channel attacks [5, 35, 46] on the TEE. Such attacks and their mitigations [36, 43] are outside the scope of this work. [...]

$$M = C^{d} \bmod n$$


M = C^d mod n
1 1 0 0 1 1 0 ···
Result = C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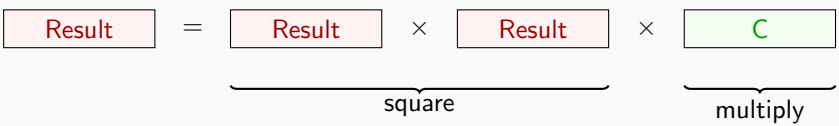
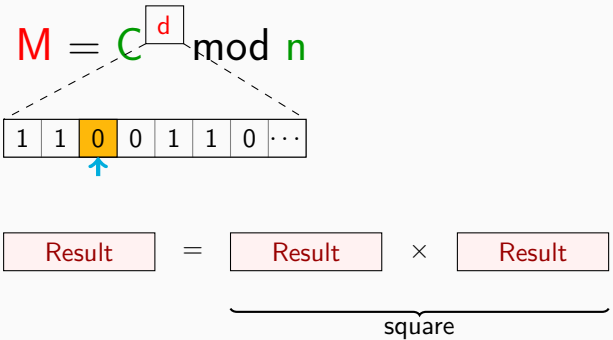

Result = Result × Result × C
square
multiply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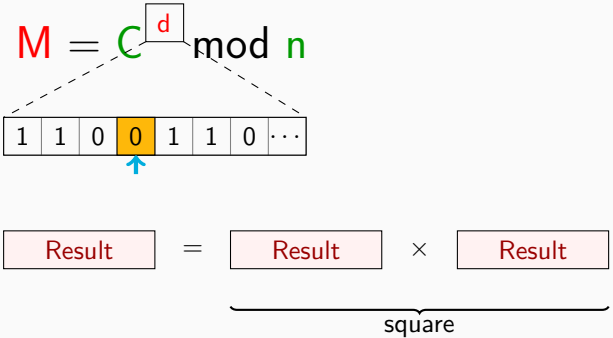
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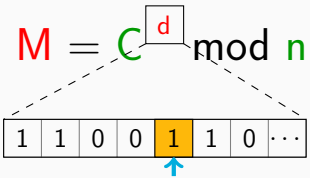
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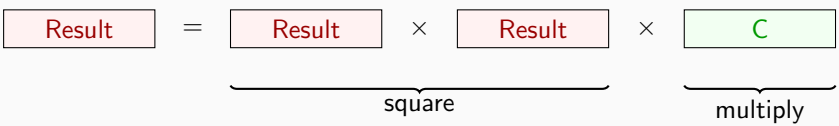
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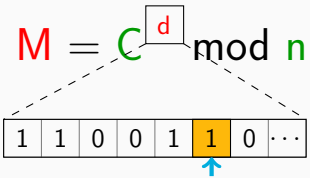
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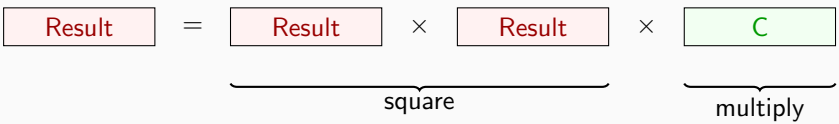
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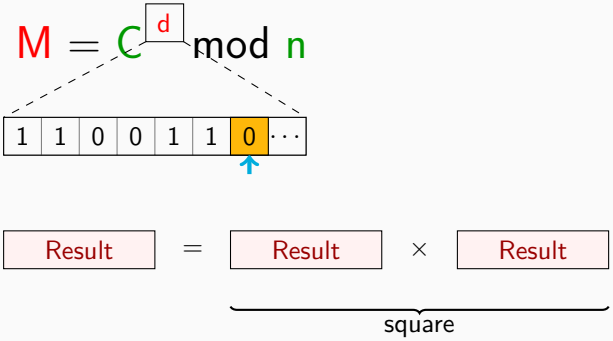
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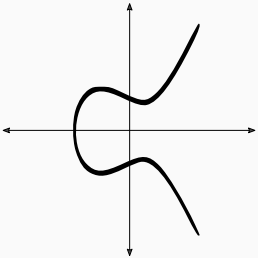
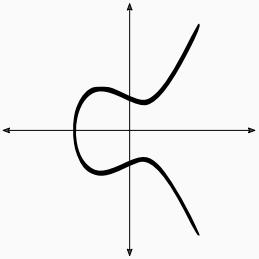
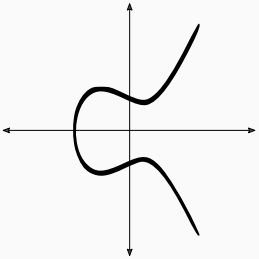


- Used to sign transactions



- Used to sign transactions
- Point multiplication is similar to RSA exponentiation



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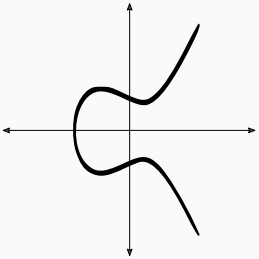
- Simplest implemention double-and-add or constant-time Montgomery ladder



- Used to sign transactions
- Point multiplication is similar to RSA exponentiation
- Simplest implemention double-and-add or constant-time Montgomery ladder
- Both algorithms have secret-dependent memory accesses

Prime+Probe [OST06; Liu+15; Mau+17]...

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- exploits the timing difference when accessing...

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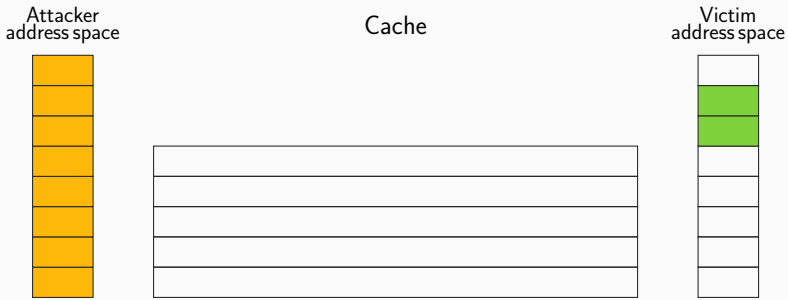
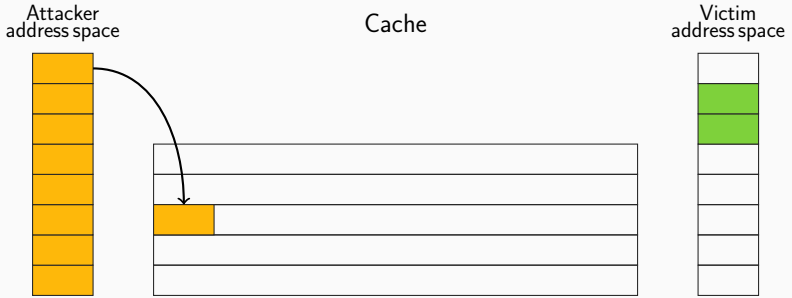
- is used to attack secret-dependent memory accesses
- is applied to a part of the CPU cache, a cache set

Prime+Probe [OST06; Liu+15; Mau+17]...

- exploits the timing difference when accessing...
  - cached data (fast)
  - uncached data (slow)
- is used to attack secret-dependent memory accesses
- is applied to a part of the CPU cache, a cache set
- works across CPU cores as the last-level cache is shared



Step 0: Attacker fills the cache (prime)



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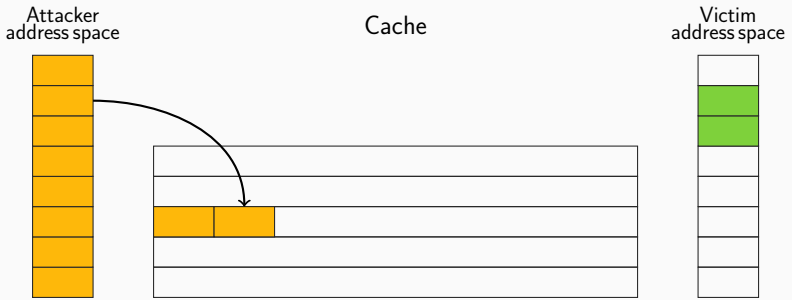

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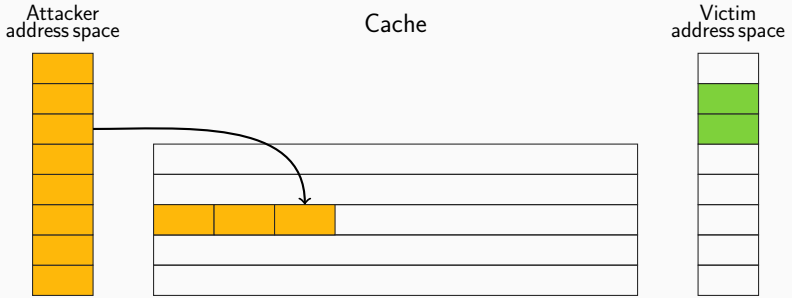

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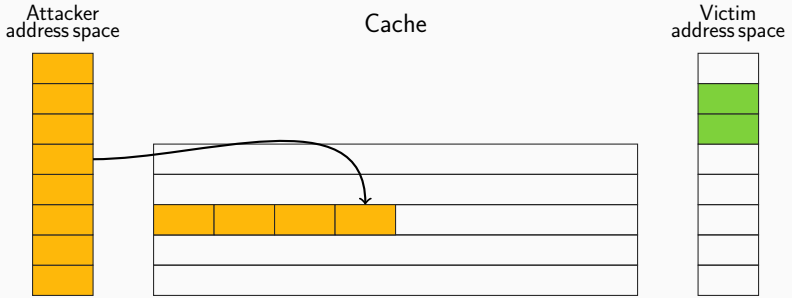

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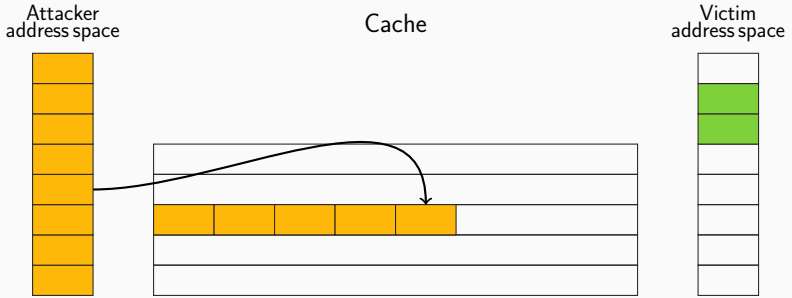

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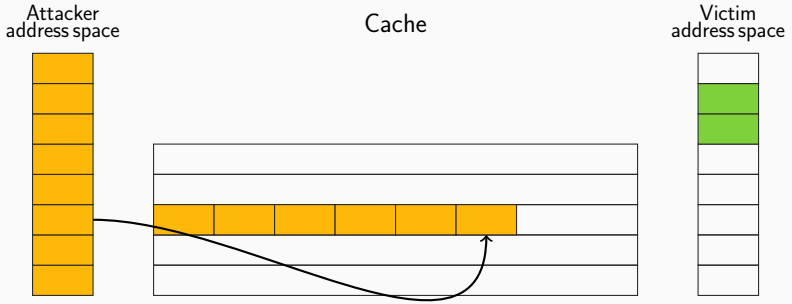

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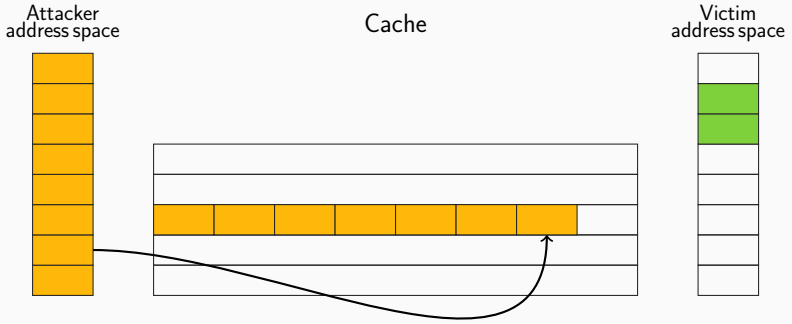

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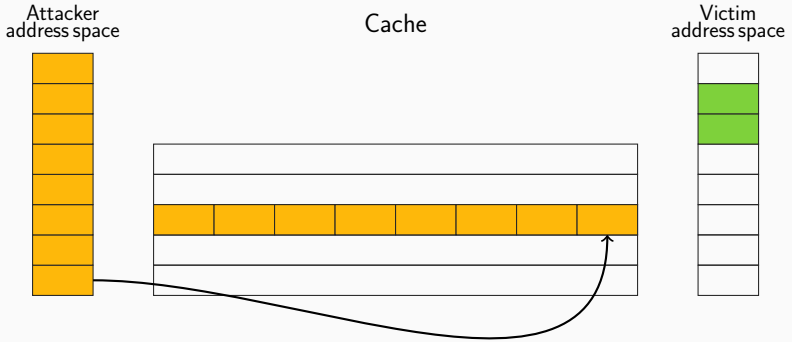

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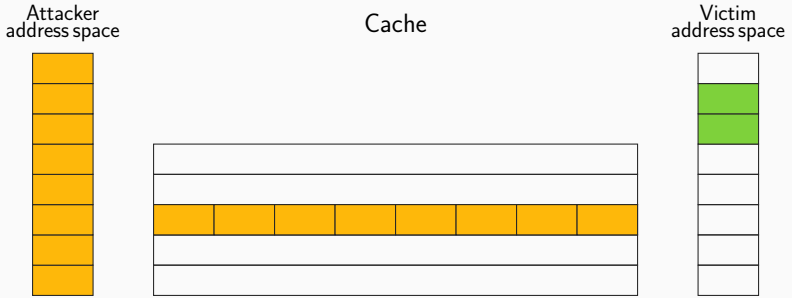

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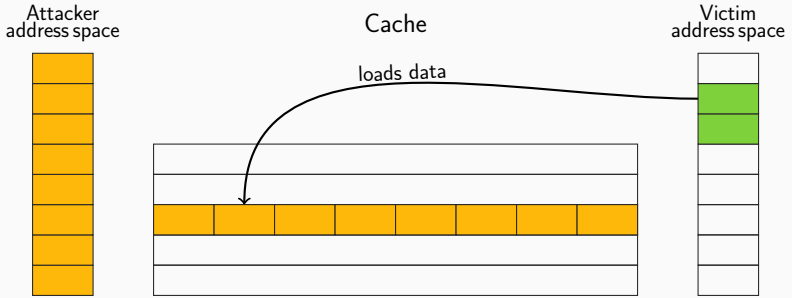

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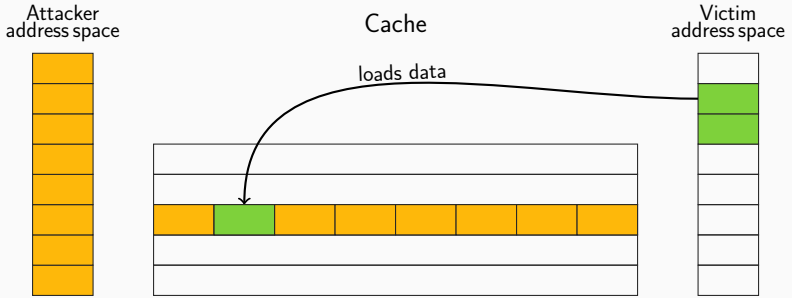
Step 1: Victim evicts cache lines by accessing own data



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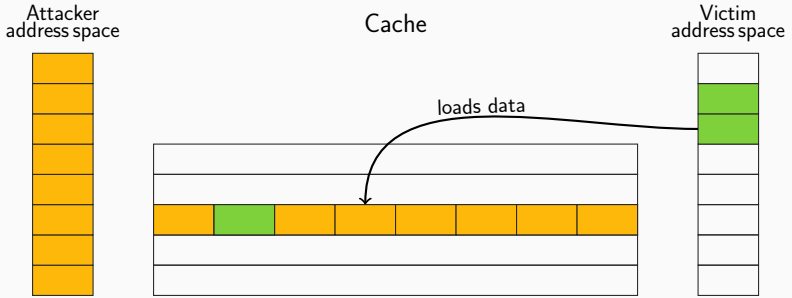

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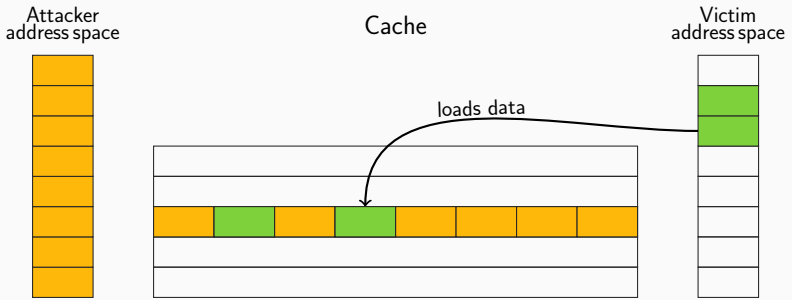

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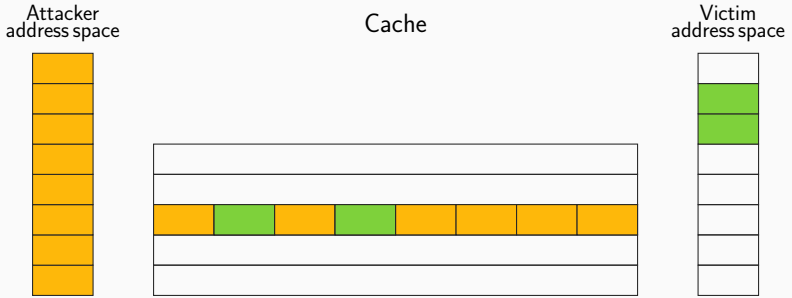

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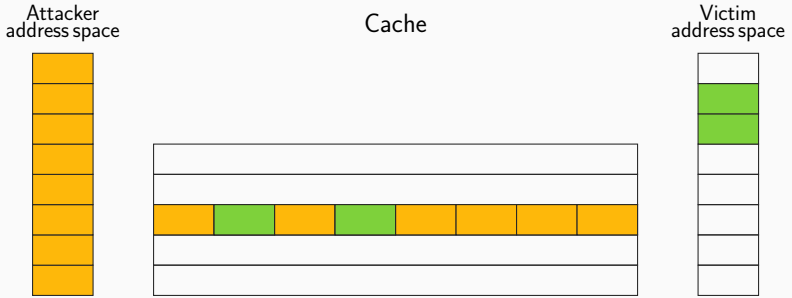

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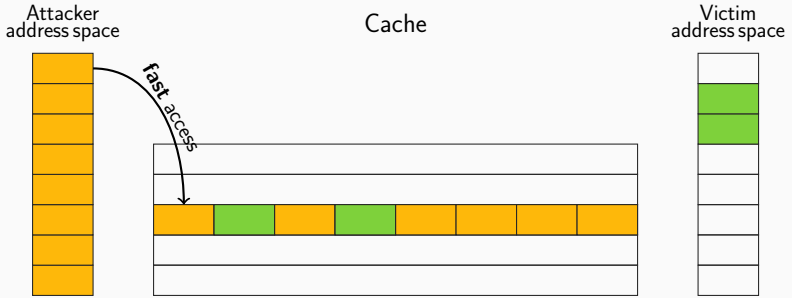
Step 2: Attacker probes data to determine if the set was accessed



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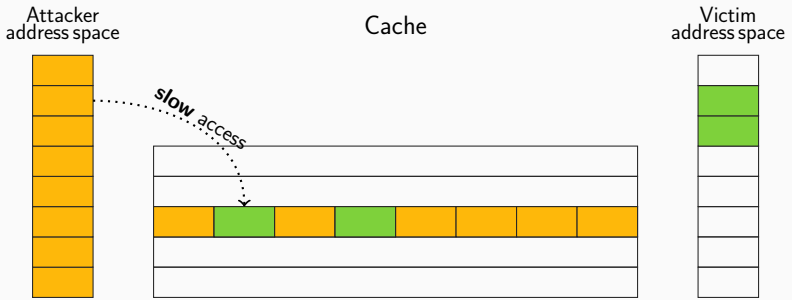


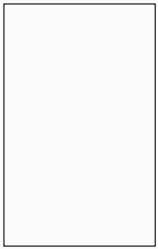
Step 0: Attacker fills the cache (prime)

Step 1: Victim evicts cache lines by accessing own data

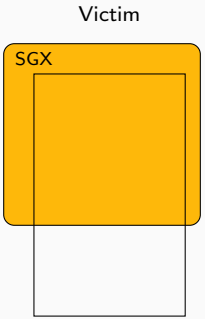
Step 2: Attacker probes data to determine if the set was accessed

Attack

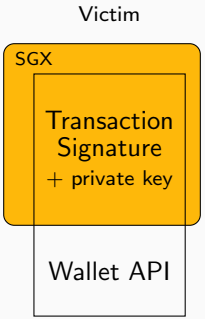
Victim

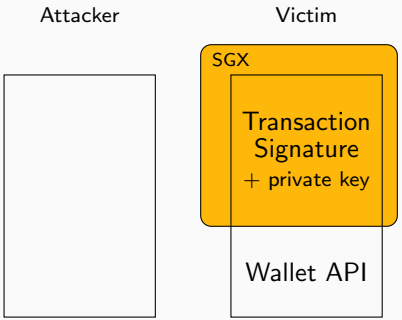


Attack Settings

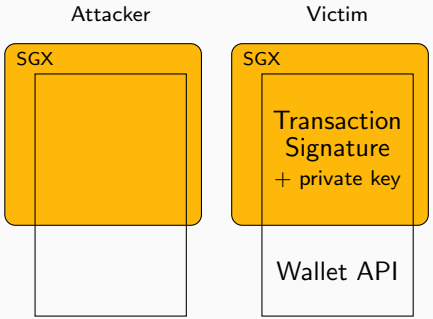


Attack Settings

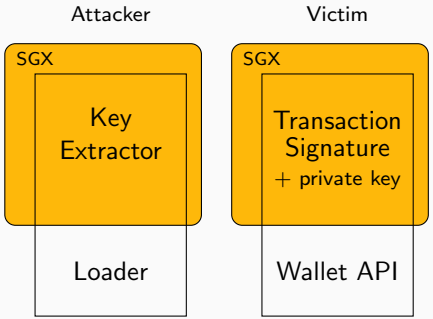



Attacker
Victim
SGX
Transaction
Signature
+ private key
Wallet API

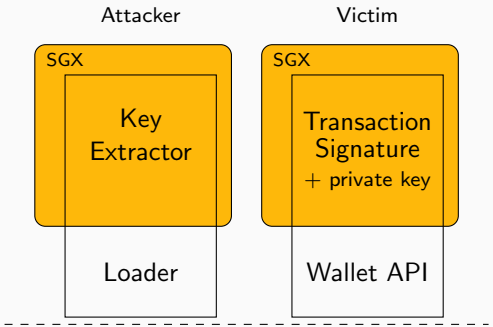
Attack Settings

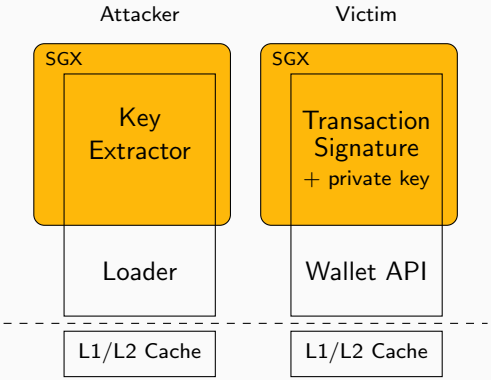


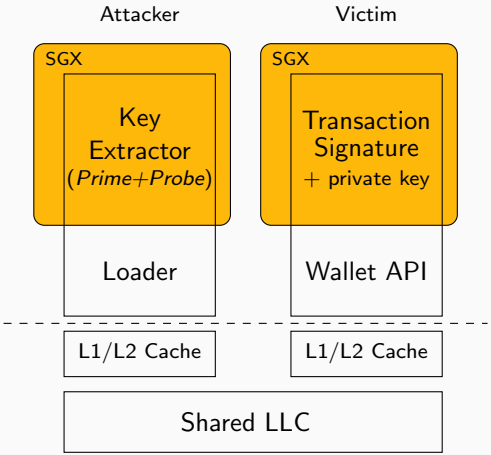
Attack Settings



Attack Settings




Attacker
Victim
SGX
Key Extractor
Loader
SGX
Transaction Signature
+ private key
Wallet API
L1/L2 Cache
L1/L2 Cache


Attacker
Victim
SGX
Key Extractor (*Prime+Probe*)
SGX
Transaction Signature + private key
Loader
Wallet API
L1/L2 Cache
L1/L2 Cache
Shared LLC

Classical Prime+Probe cannot be mounted within SGX:

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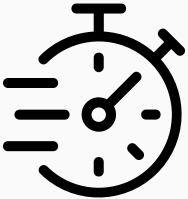
Classical Prime+Probe cannot be mounted within SGX:

- No access to high-precision timer (`rdtsc`)
- No syscalls
- No shared memory
- No physical addresses
- No 2 MB large pages

- We have to build our own timer



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- We have to build our own timer
- Timer resolution must be in the order of cycles
- Start a thread that continuously increments a global variable
- The global variable is our timestamp

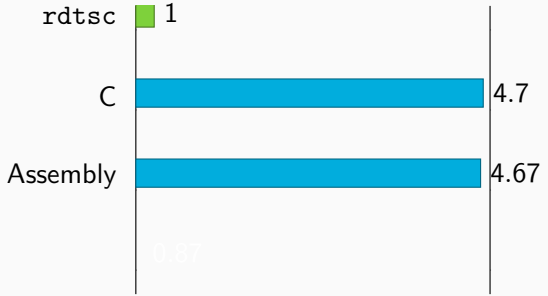
CPU cycles one increment takes


```
1 timestamp = rdtsc();
```

CPU cycles one increment takes

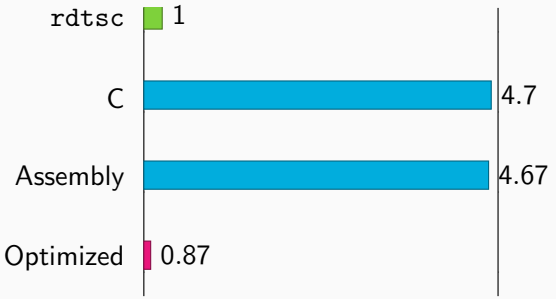

```
1 while(1) {
2   timestamp++;
3 }
```

CPU cycles one increment takes

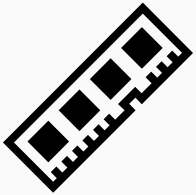



```
1 mov &timestamp, %rcx
2 1: incl (%rcx)
3 jmp 1b
```

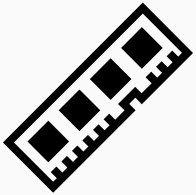
CPU cycles one increment takes



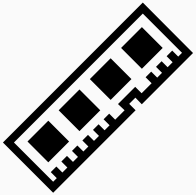

```
1 mov &timestamp, %rcx
2 1: inc %rax
3 mov %rax, (%rcx)
4 jmp 1b
```



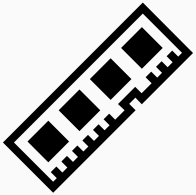
- Cache set is determined by part of physical address [Mau+15]



- Cache set is determined by part of physical address [Mau+15]
- We have no knowledge of physical addresses



- Cache set is determined by part of physical address [Mau+15]
- We have no knowledge of physical addresses
- Use the reverse-engineered DRAM mapping [Pes+16]



- Cache set is determined by part of physical address [Mau+15]
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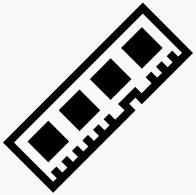
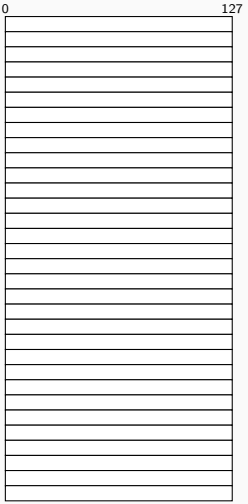
- Exploit timing differences to find DRAM row borders



- Cache set is determined by part of physical address [Mau+15]
- We have no knowledge of physical addresses
- Use the reverse-engineered DRAM mapping [Pes+16]
- Exploit timing differences to find DRAM row borders
- The 18 LSBs are '0' at a row border

Physical Addresses

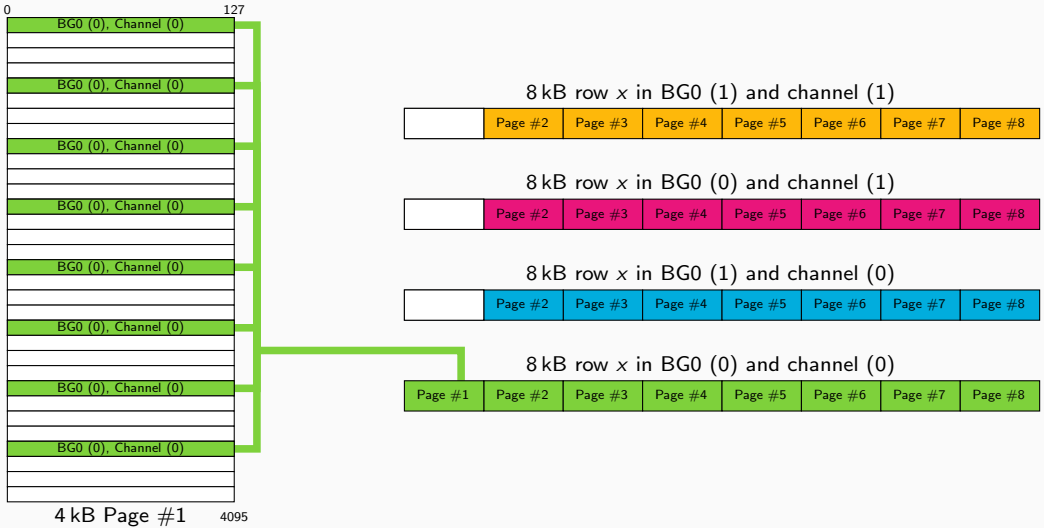


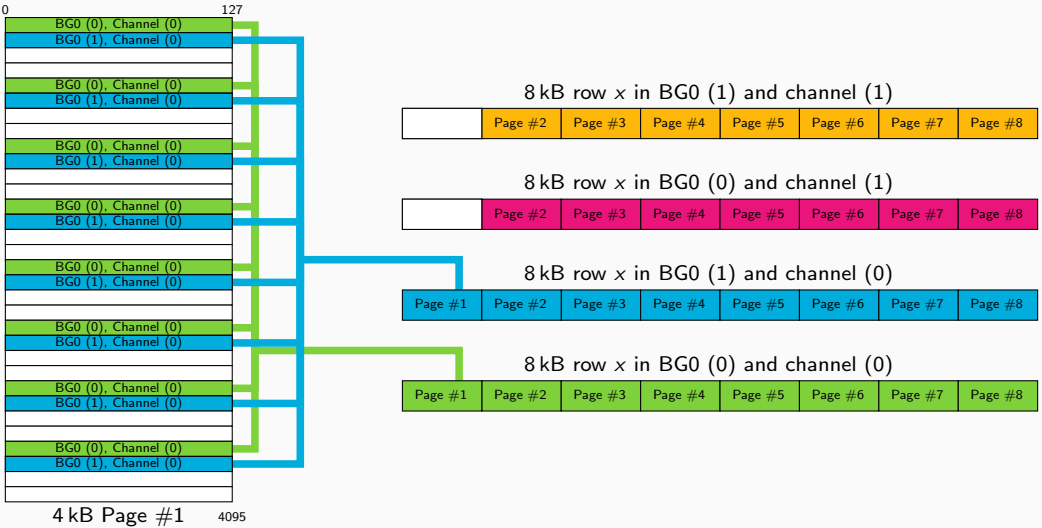
8 kB row x in BG0 (1) and channel (1)

8 kB row x in BG0 (0) and channel (1)

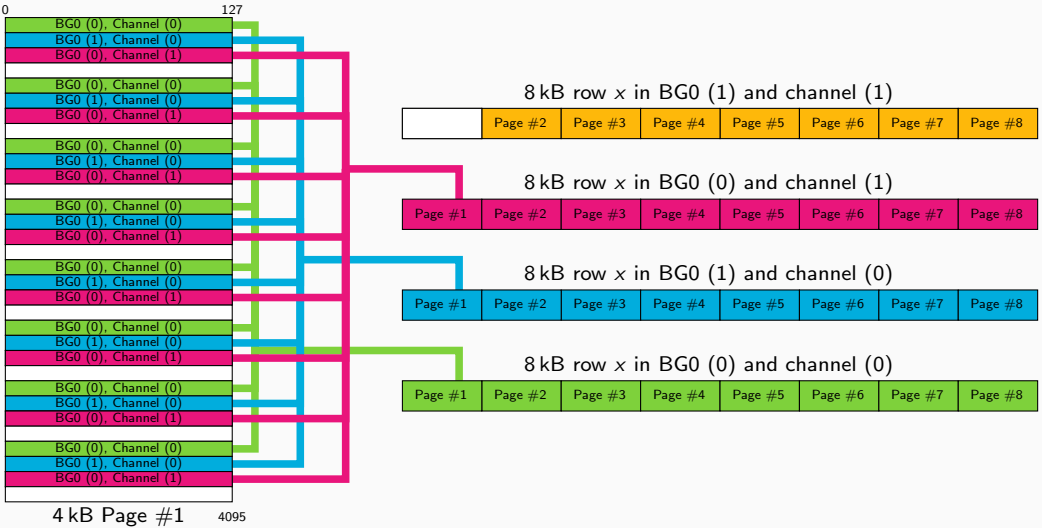
8 kB row x in BG0 (1) and channel (0)

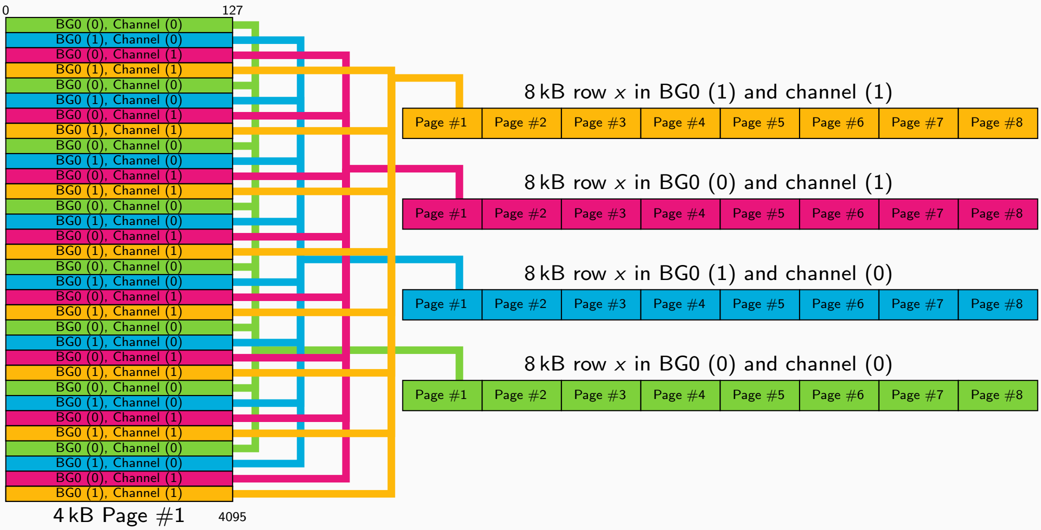
8 kB row x in BG0 (0) and channel (0)


0
127
BG0 (0), Channel (0)
BG0 (0), Channel (0)
BG0 (0), Channel (0)
BG0 (0), Channel (0)
BG0 (0), Channel (0)
BG0 (0), Channel (0)
BG0 (0), Channel (0)
BG0 (0), Channel (0)
4 kB Page #1
4095
8 kB row x in BG0 (1) and channel (1)
Page #2
Page #3
Page #4
Page #5
Page #6
Page #7
Page #8
8 kB row x in BG0 (0) and channel (1)
Page #2
Page #3
Page #4
Page #5
Page #6
Page #7
Page #8
8 kB row x in BG0 (1) and channel (0)
Page #2
Page #3
Page #4
Page #5
Page #6
Page #7
Page #8
8 kB row x in BG0 (0) and channel (0)
Page #1
Page #2
Page #3
Page #4
Page #5
Page #6
Page #7
Page #8


0
127
BG0 (0), Channel (0)
BG0 (1), Channel (0)
4 kB Page #1
4095
8 kB row x in BG0 (1) and channel (1)
Page #2
Page #3
Page #4
Page #5
Page #6
Page #7
Page #8
8 kB row x in BG0 (0) and channel (1)
8 kB row x in BG0 (1) and channel (0)
Page #1
8 kB row x in BG0 (0) and channel (0)

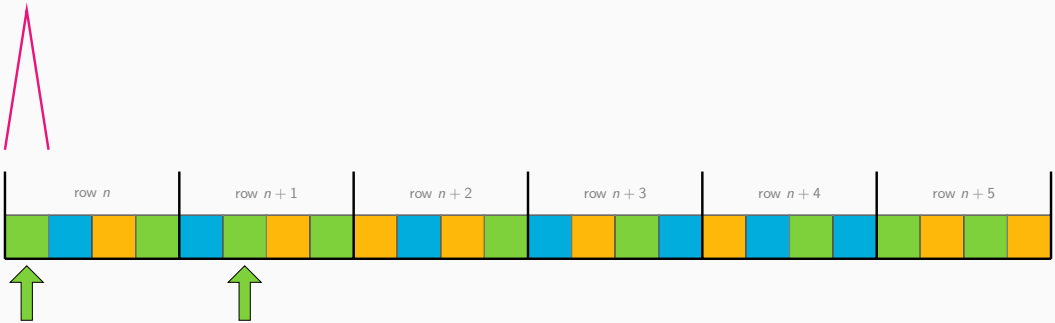
Physical Addresses



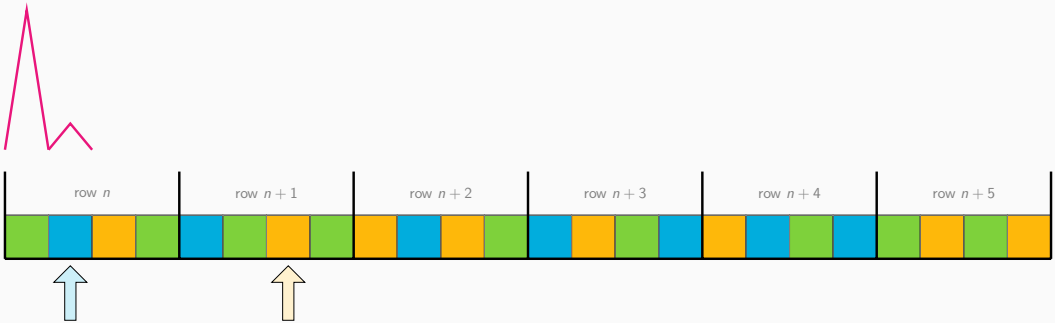


0
127
BG0 (0), Channel (0)
BG0 (1), Channel (0)
BG0 (0), Channel (1)
BG0 (1), Channel (1)
4 kB Page #1
4095
8 kB row x in BG0 (1) and channel (1)
Page #1 Page #2 Page #3 Page #4 Page #5 Page #6 Page #7 Page #8
8 kB row x in BG0 (0) and channel (1)
Page #1 Page #2 Page #3 Page #4 Page #5 Page #6 Page #7 Page #8
8 kB row x in BG0 (1) and channel (0)
Page #1 Page #2 Page #3 Page #4 Page #5 Page #6 Page #7 Page #8
8 kB row x in BG0 (0) and channel (0)
Page #1 Page #2 Page #3 Page #4 Page #5 Page #6 Page #7 Page #8

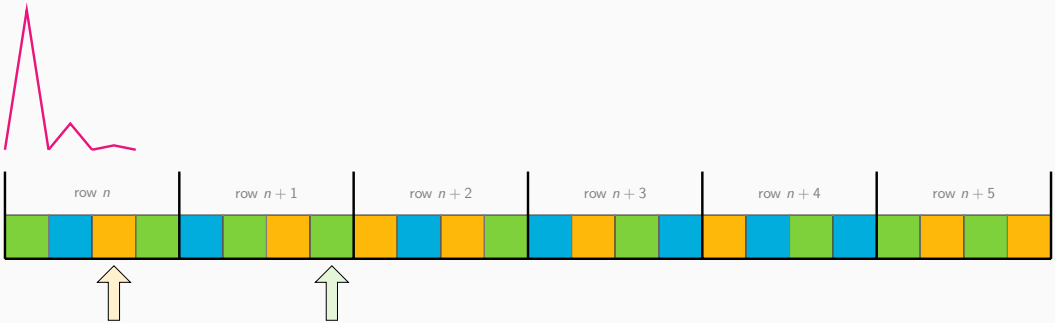
Physical Addresses



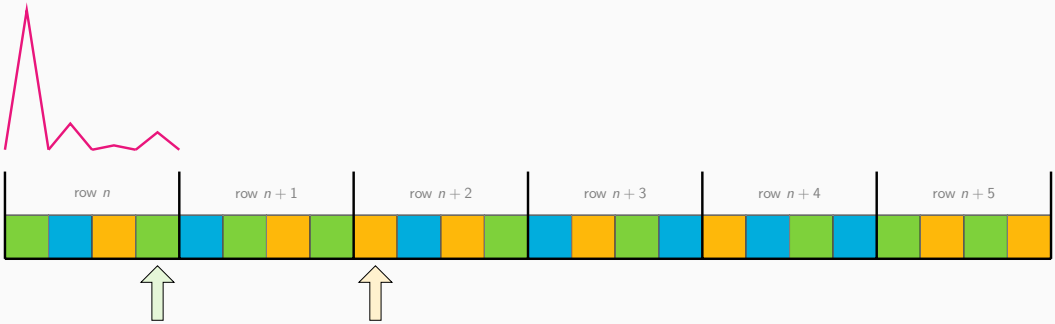
Physical Addresses



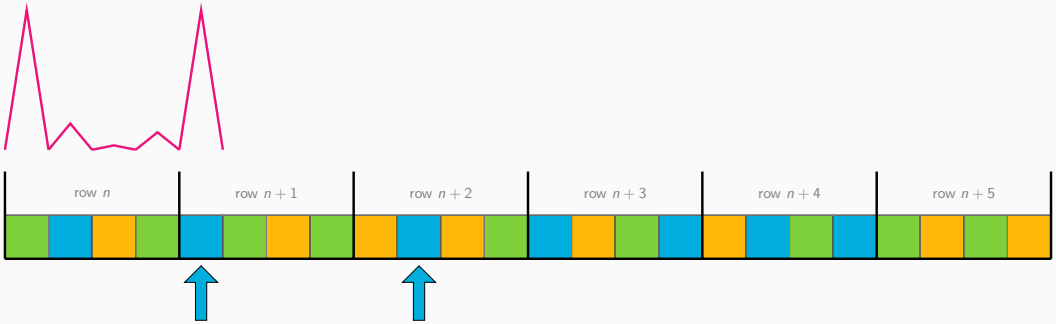
Physical Addresses

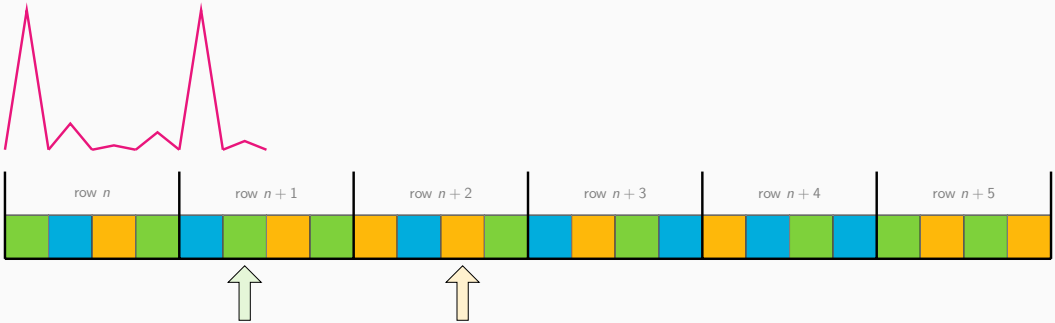


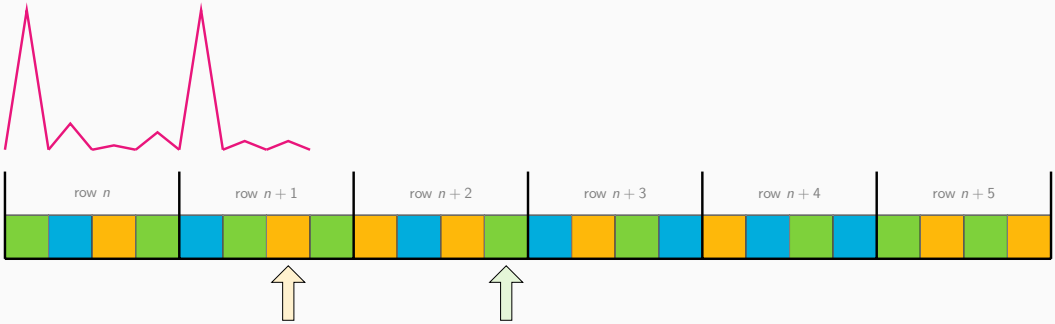
Physical Addresses



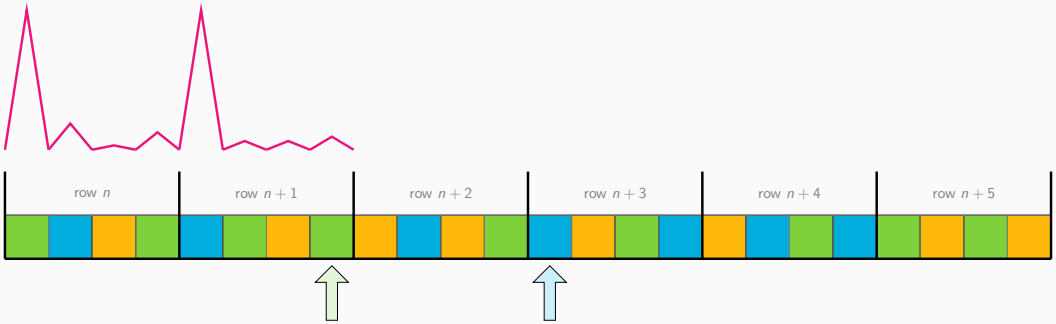
Physical Addresses

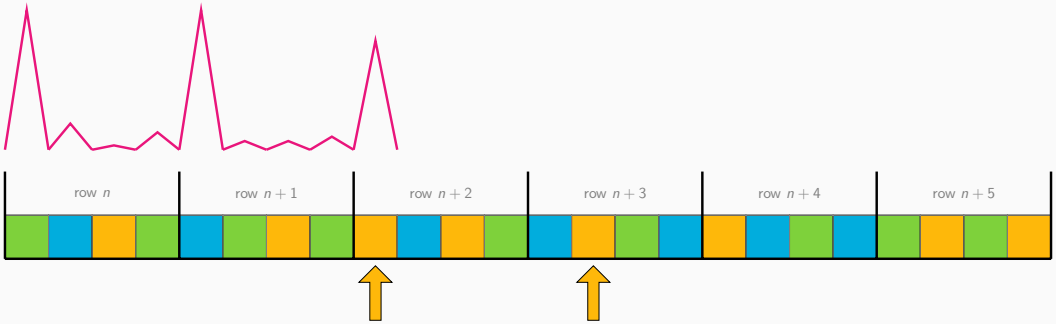



row n
row $n+1$
row $n+2$
row $n+3$
row $n+4$
row $n+5$


row n
row $n+1$
row $n+2$
row $n+3$
row $n+4$
row $n+5$

Physical Addresses




row n
row $n+1$
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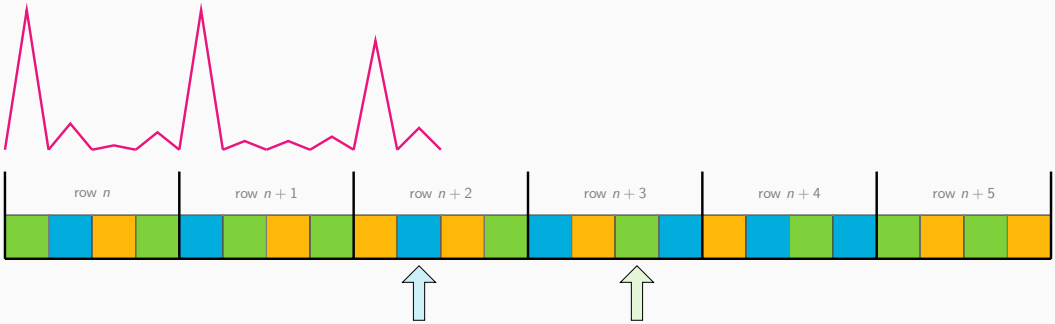
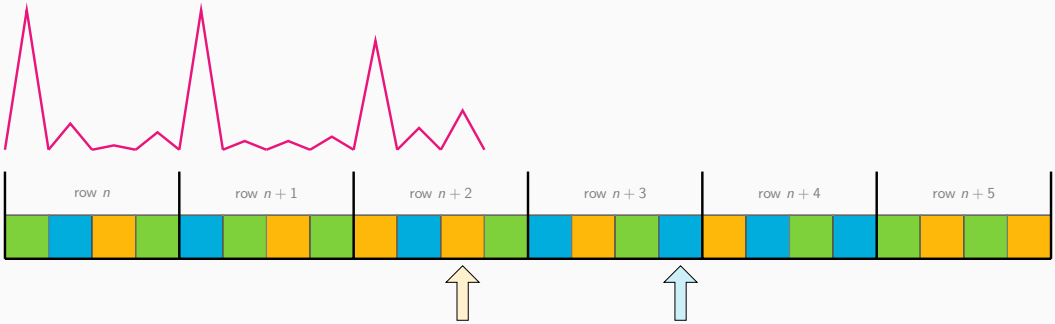
row $n+4$
row $n+5$

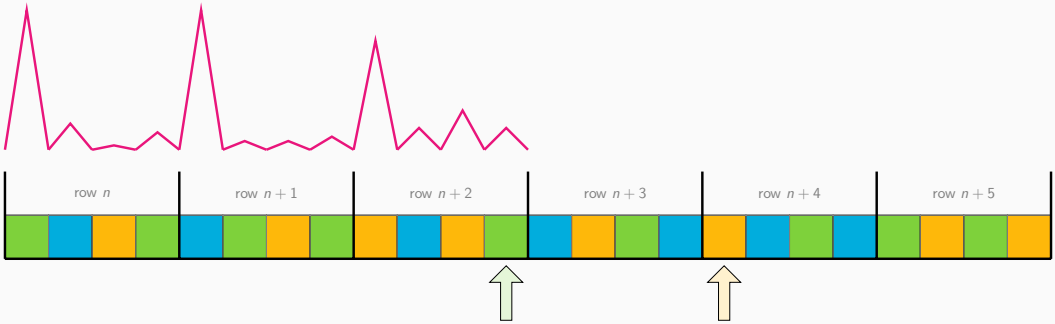
Physical Addresses



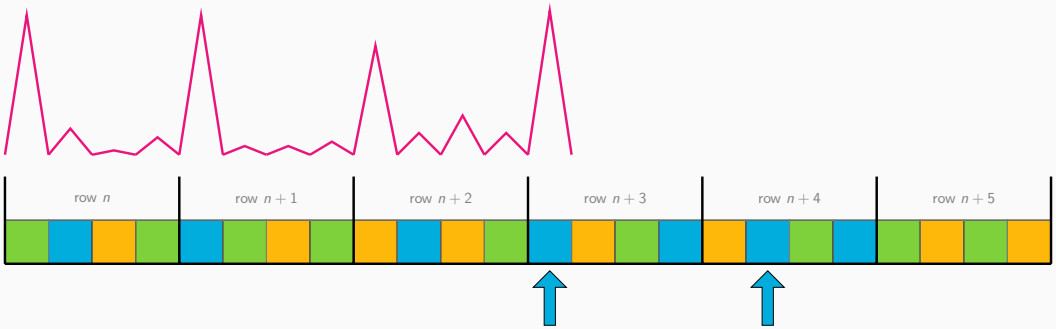
Physical Addresses



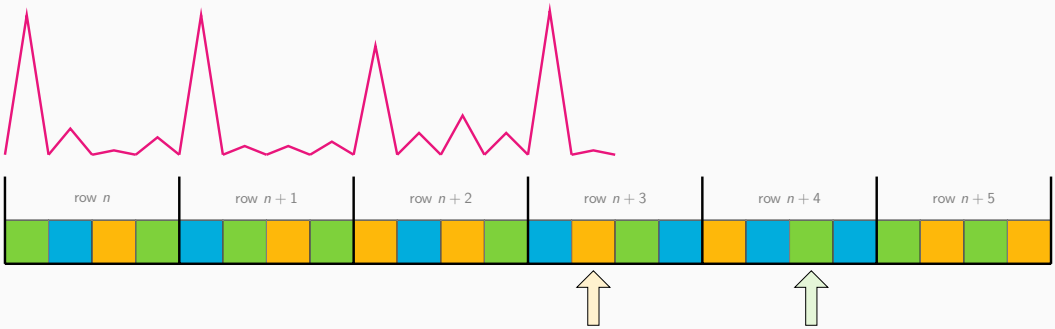
Physical Addresses



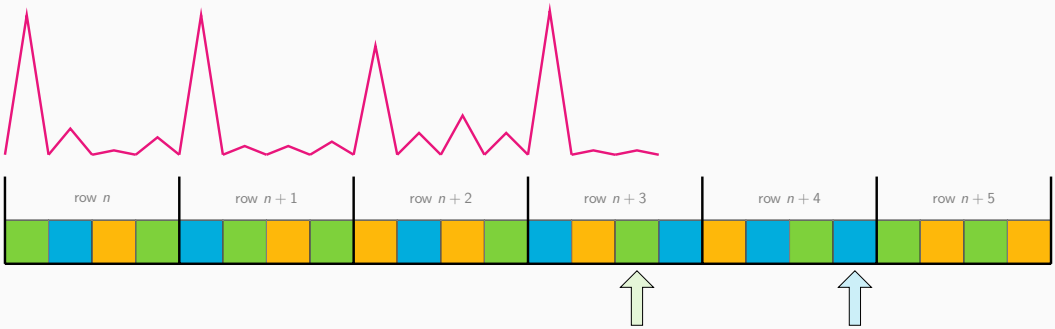
Physical Addresses

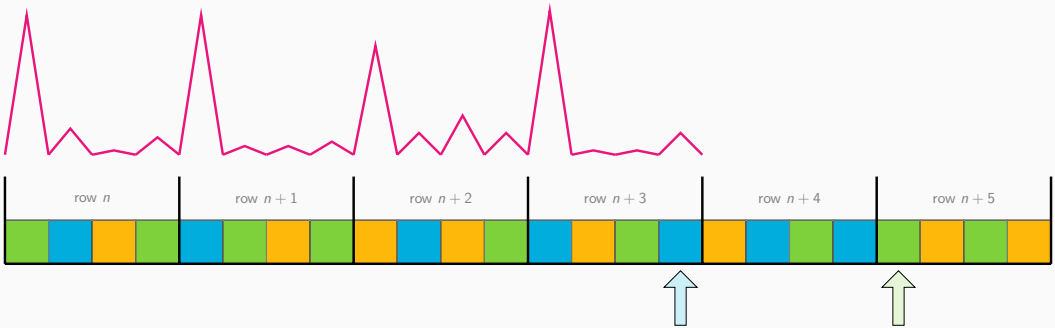


Physical Addresses

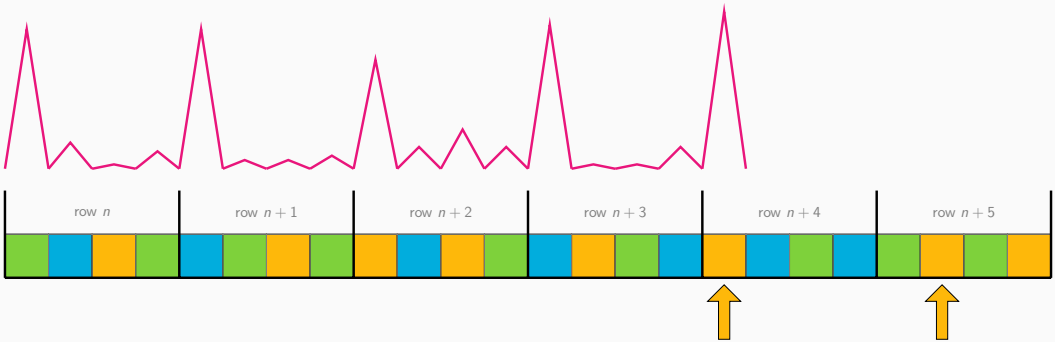


Physical Addresses

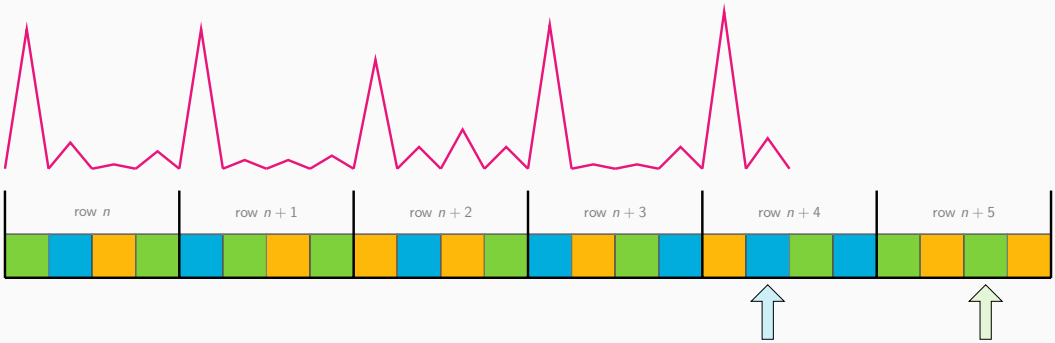



row n
row $n+1$
row $n+2$
row $n+3$
row $n+4$
row $n+5$

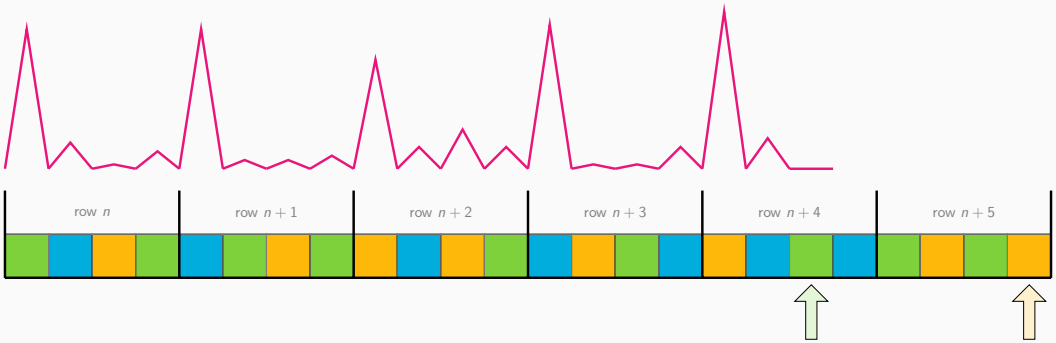
Physical Addresses



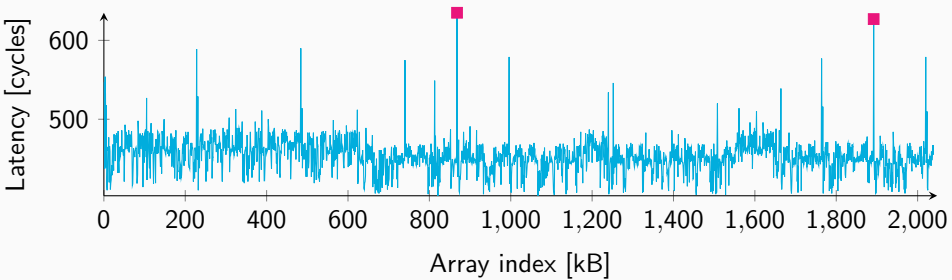
Physical Addresses

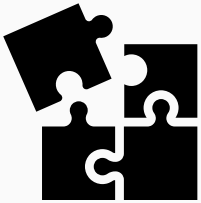


Physical Addresses



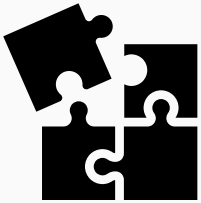
Result on an Intel i5-6200U





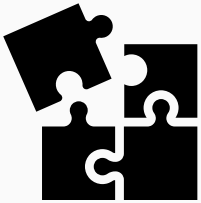
1. Use the counting primitive to measure DRAM accesses

Combining Everything

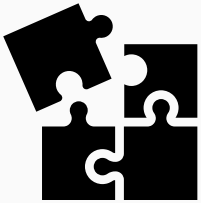


1. Use the counting primitive to measure DRAM accesses
2. Through the DRAM side channel, determine the row borders

Combining Everything



1. Use the counting primitive to measure DRAM accesses
2. Through the DRAM side channel, determine the row borders
3. Row borders have the 18 LSBs set to '0' $\rightarrow$ maps to cache set '0'



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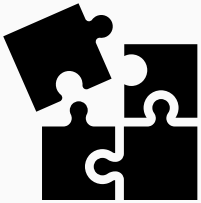
Combining Everything



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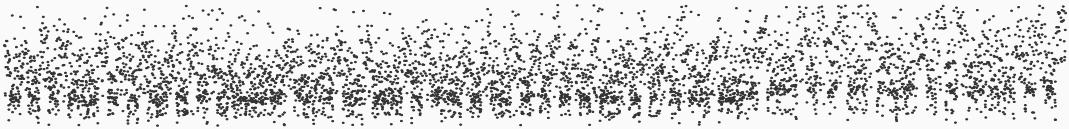
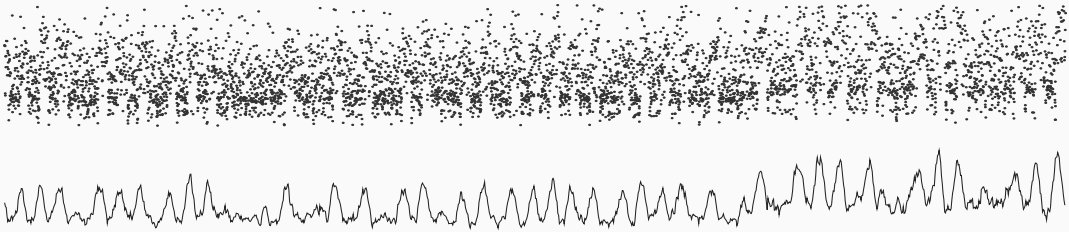
5. Mount Prime+Probe on the buffer containing the multiplier [Sch+17]

Results

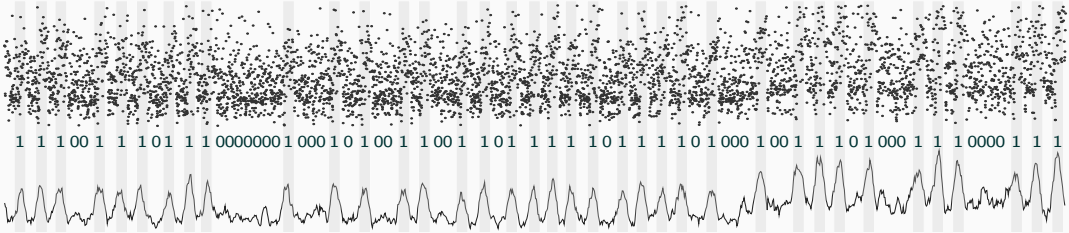
Raw Prime+Probe trace...

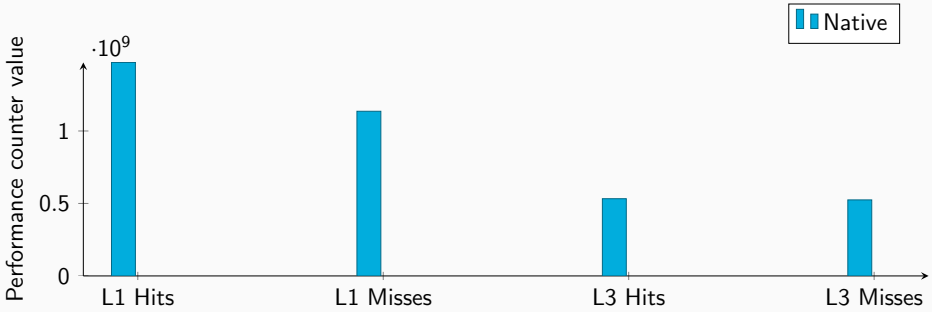


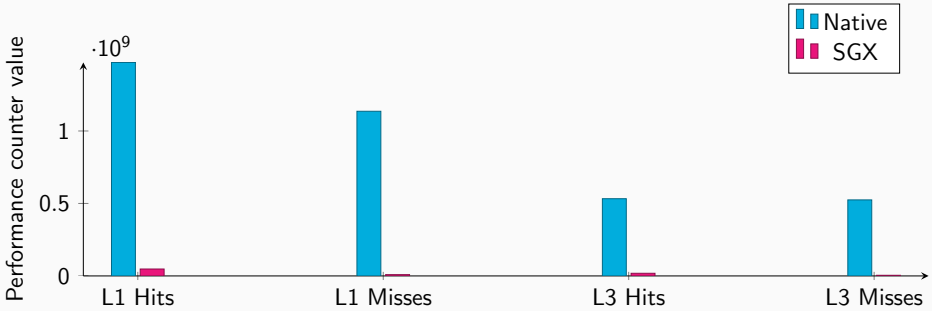
...processed with a simple moving average...



...allows to clearly see the bits of the exponent




Native
Performance counter value
$\cdot 10^9$
1
0.5
0
L1 Hits
L1 Misses
L3 Hits
L3 Misses


Native
SGX
Performance counter value
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0.5
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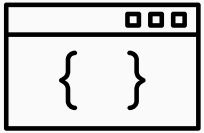
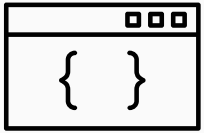
Countermeasures



- Cache attacks can be prevented on source level



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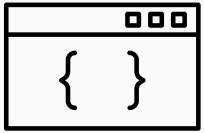

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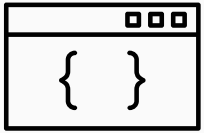

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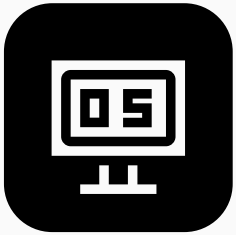
- Bit-sliced implementations are not vulnerable to cache attacks



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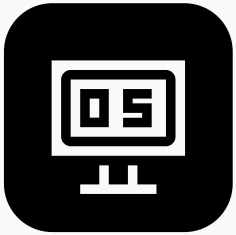

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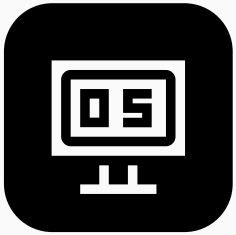

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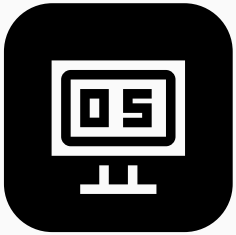

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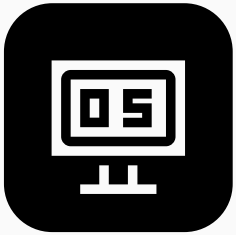

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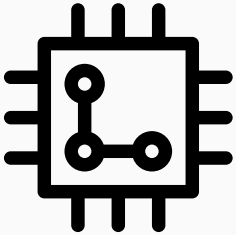

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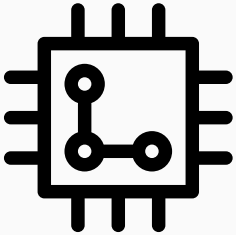

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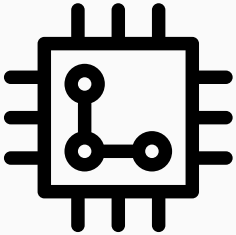

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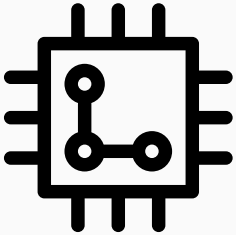

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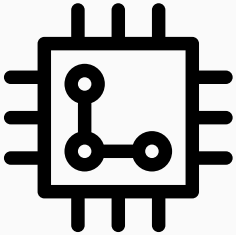

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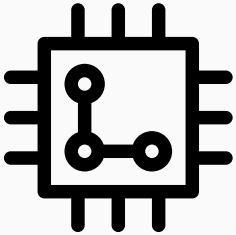

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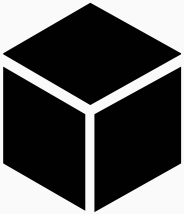
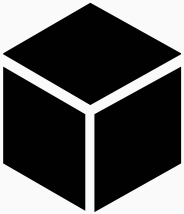
- Provide a non-shared secure memory element which is not cached

Exploiting Non-Side-Channel Bugs using Side-Channel Attacks



- Assuming a side-channel resistant crypto implementation



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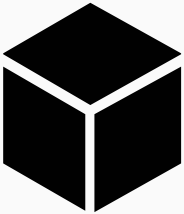

- Assuming a side-channel resistant crypto implementation
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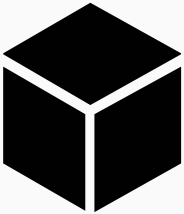

- Assuming a side-channel resistant crypto implementation
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- No source or (unencrypted) binary available
- A blackbox with an API


DRM
Video
Player

- A classical digitial rights management scenario

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- Plays the file, e.g., using Intel's Protected Audio Video Path (PAVP)

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- ...not pay for the same movie over and over

- We do not like DRM
- And we want to keep our stolen Bitcoins...
- ...not pay for the same movie over and over
- No cache attack on crypto this time

A Glance at the Code

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void play_file(DRMFile* file) {
  if(check_signature(file->header) == ERR_INVALID) {
    // invalid signature
    return;
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DRM-protected file

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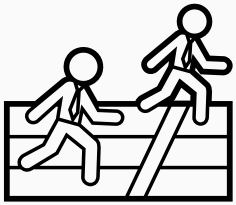
Everything is fine



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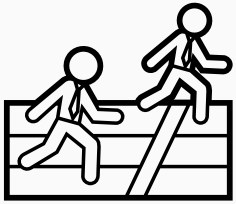

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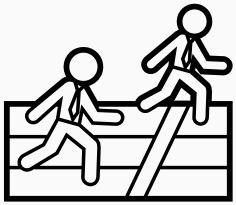
A Race Condition



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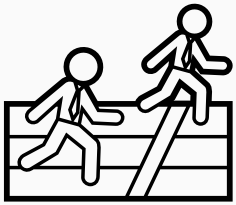

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- This can create race conditions

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Shared memory

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Shared memory

First access of shared memory

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Shared memory

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Second access of shared memory

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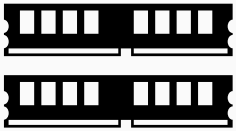
Shared memory

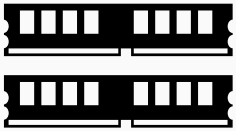
First access of shared memory

Headers can be changed here!

Second access of shared memory



- A time-of-check-to-time-of-use (TOCTTOU) bug



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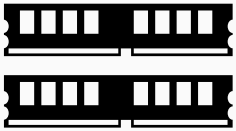

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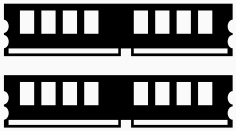

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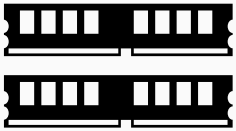

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- Caused by accessing the shared memory twice
- Also called double-fetch bugs

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- What if we have neither code nor binary?

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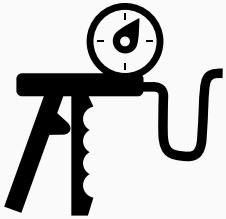
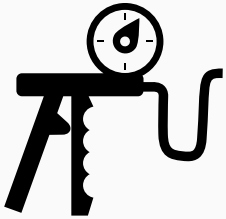
- Memory accesses are visible in the cache
- Observe memory accesses via cache attack



- Shared memory makes it a lot easier



- Shared memory makes it a lot easier
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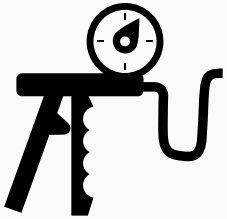

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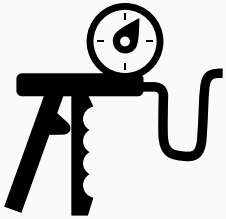

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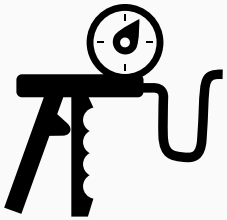
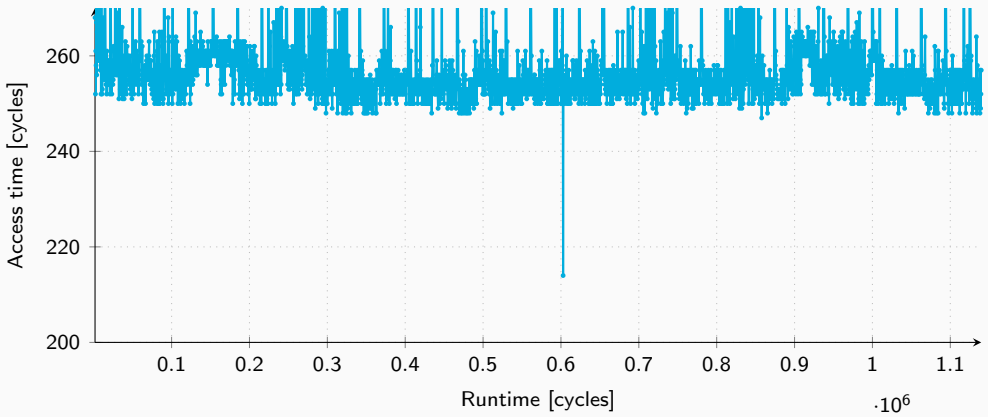
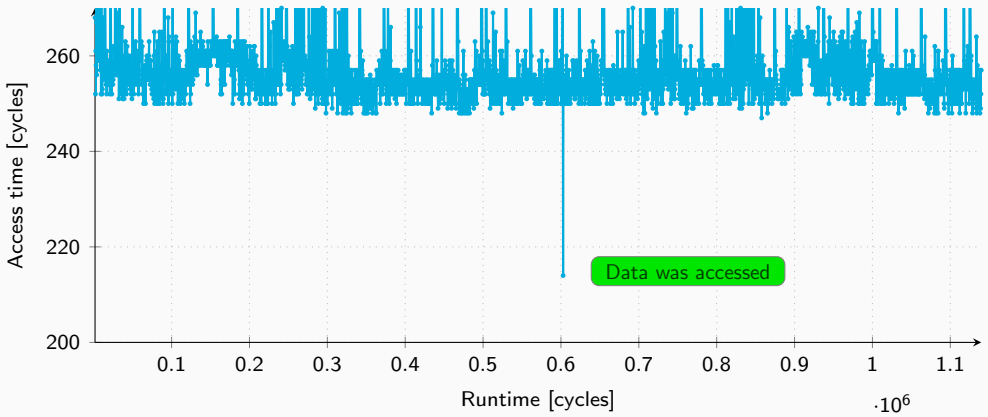


- Shared memory makes it a lot easier
- Constantly flush value from cache using `clflush` instruction
- Schedule victim
- Measure access time to value
- If access is fast, victim accessed (and cached) the data


Access time [cycles]
260
240
220
200
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
1.1
Runtime [cycles]
·10^6


Access time [cycles]
260
240
220
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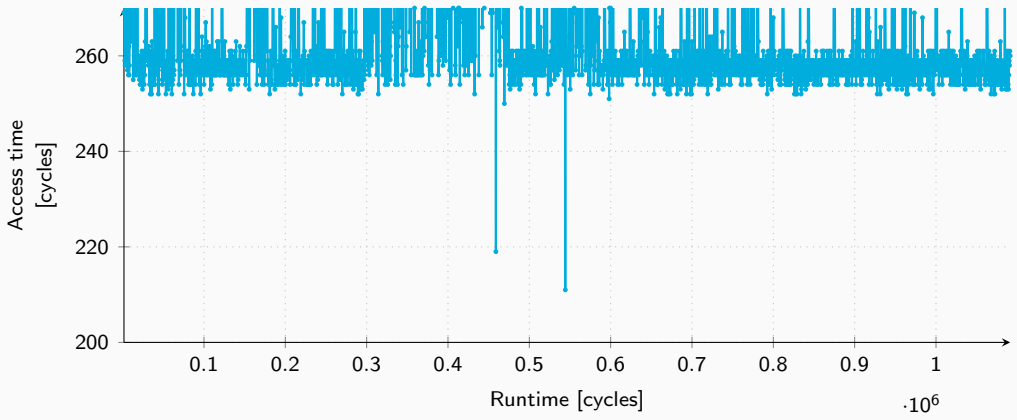
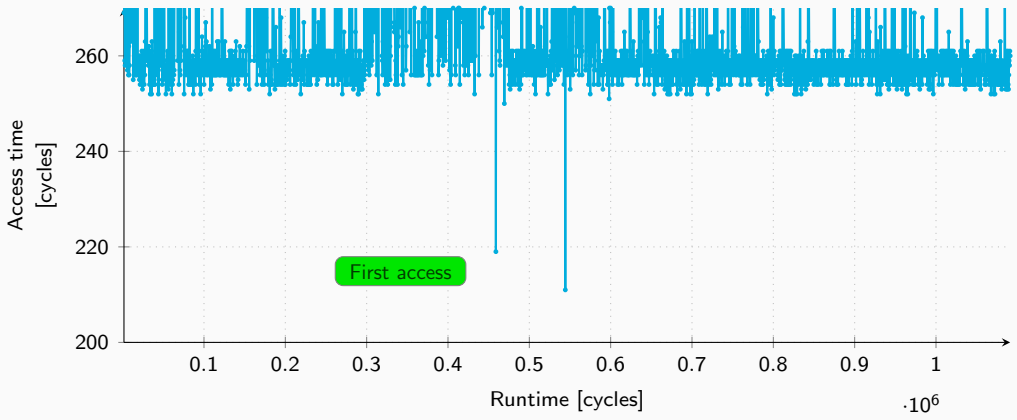
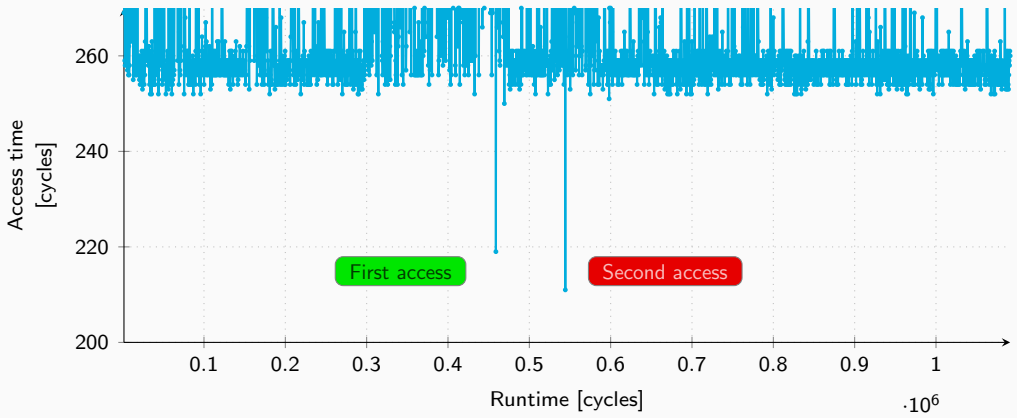
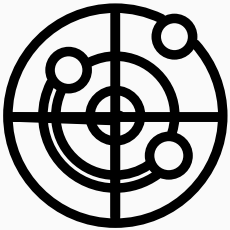
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
1.1
Runtime [cycles]
·10^6
Data was accessed

Double-fetch Detection

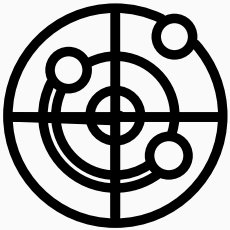



Access time [cycles]
260
240
220
200
First access
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Runtime [cycles]
·10^6


Access time [cycles]
260
240
220
200
First access
Second access
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Runtime [cycles]
·10^6



- Cache attacks dynamically detect double fetches in black boxes



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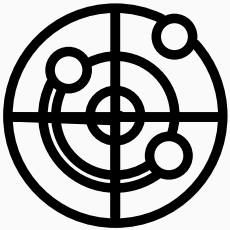

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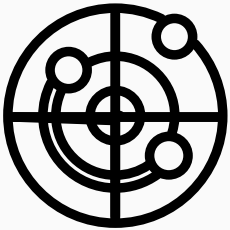

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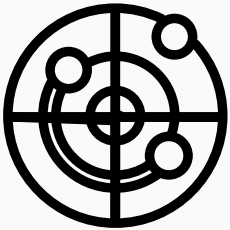

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- The further apart the two fetches, the higher the probability
- Minimum time between accesses is approximately 600 cycles
- If the time is $\geq$ 3 000 cycles, detection rate is close to 100 %
- Allows automated detection of double fetches in many scenarios

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- We need a trigger

Cache-based Trigger

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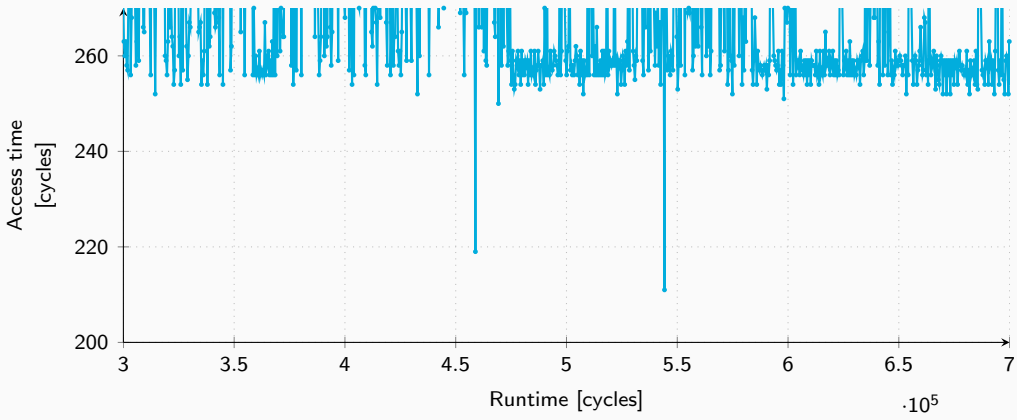
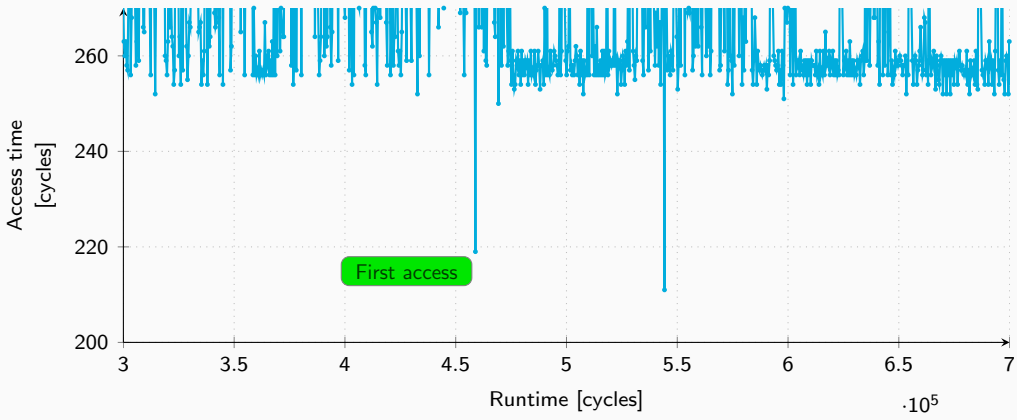
- The first memory access acts as our trigger
- Simply change the value immediately after the first access

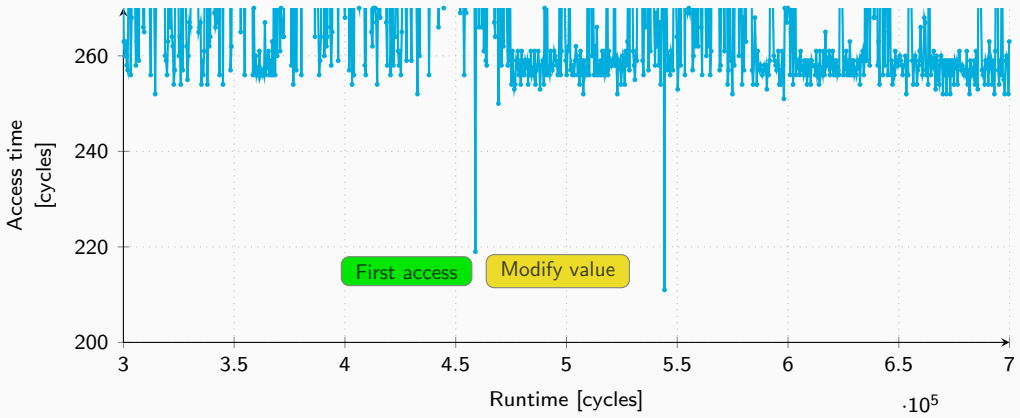
Cache-based Trigger



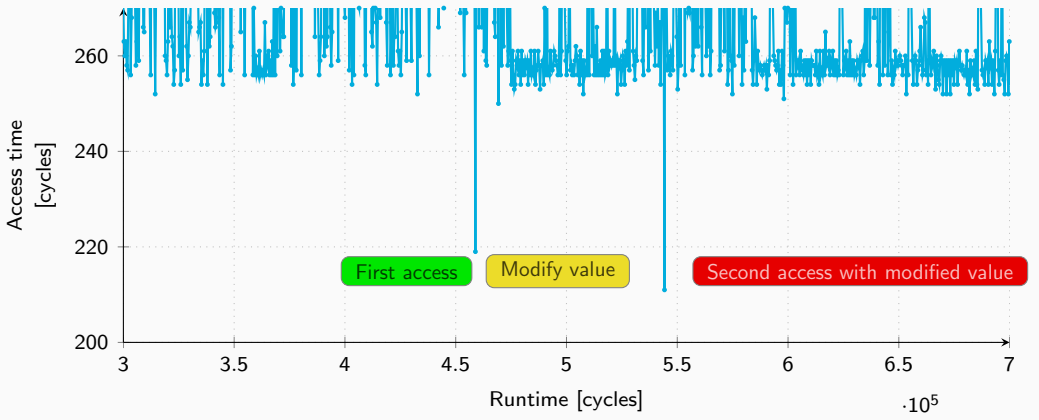
Cache-based Trigger



Cache-based Trigger



Cache-based Trigger




Live
DEMO

Preventing Exploitation of Double-fetch Bugs

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- Only problematic if a modified value leads to an exploit
- Even frameworks to exploit such race conditions [Wei+16]
- With cache trigger very reliable [Sch+18]

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- We have such a mechanism on modern Intel CPUs
- Intel TSX provides exactly this functionality in hardware

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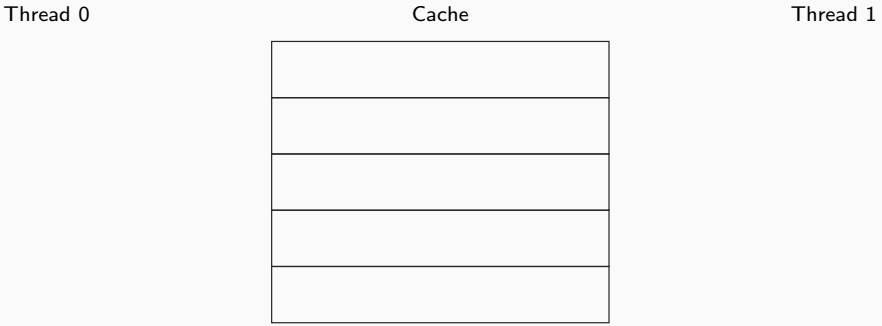
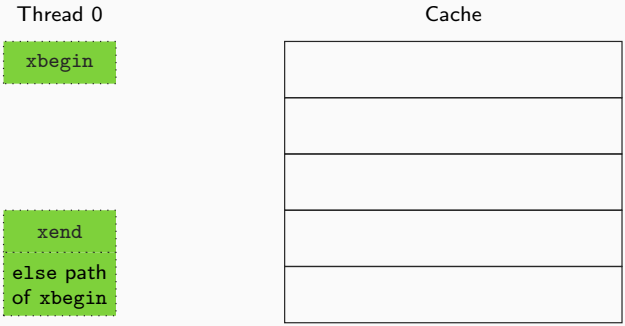
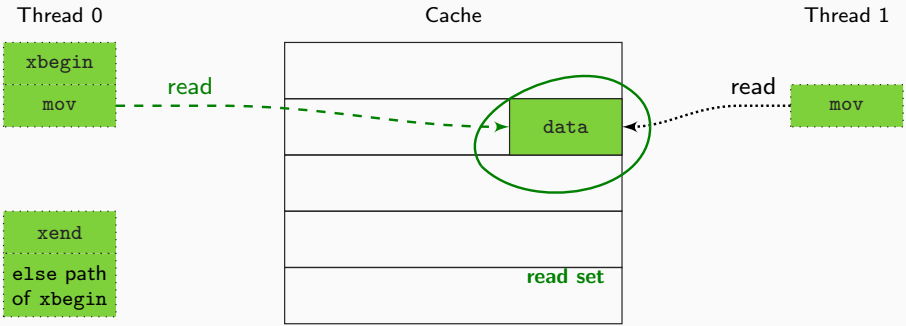
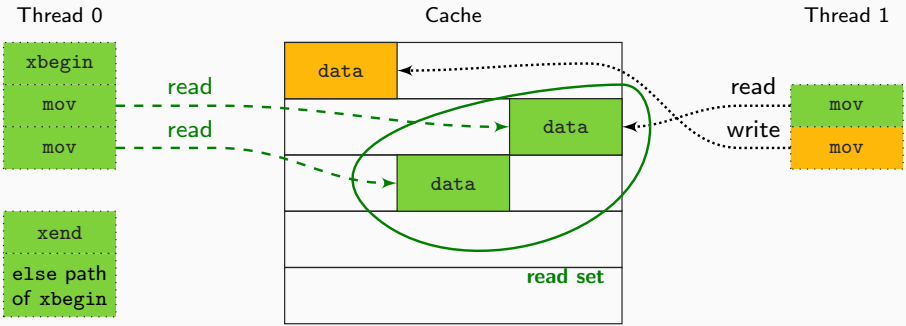
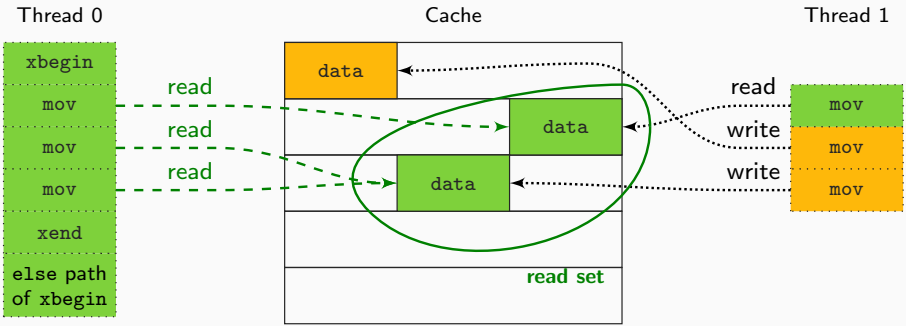
- Implemented using the cache

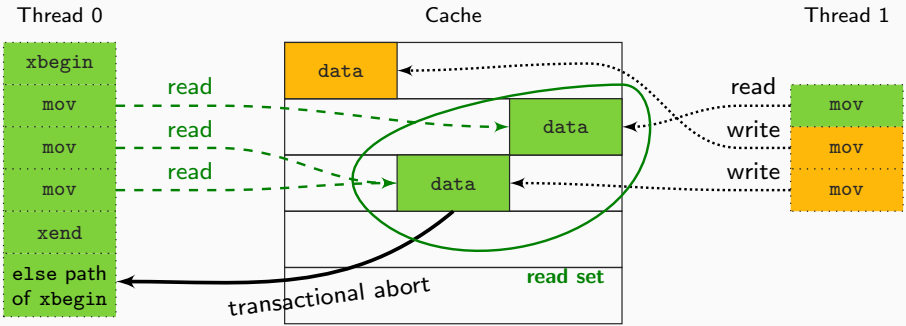

Thread 0
Cache
Thread 1

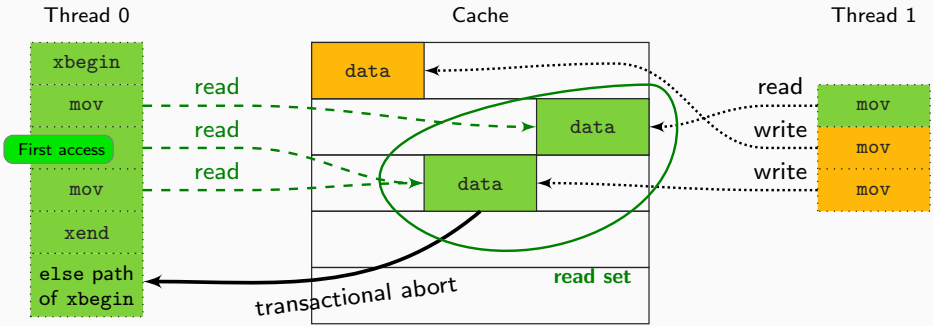

Thread 0
Cache
Thread 1
xbegin
xend
else path
of xbegin


Thread 0
Cache
Thread 1
xbegin
mov
read
data
read
mov
xend
else path
of xbegin
read set


Thread 0
Cache
Thread 1
xbegin
mov
mov
xend
else path
of xbegin
read
read
data
data
data
read set
read
write
mov
mov


Thread 0
Cache
Thread 1
xbegin
mov
mov
mov
xend
else path of xbegin
read
read
read
data
data
data
read set
read
write
write
mov
mov
mov


Thread 0
Cache
Thread 1
xbegin
mov
mov
mov
xend
else path of xbegin
read
read
read
data
data
data
read
write
write
mov
mov
mov
transactional abort
read set


Thread 0
Cache
Thread 1
xbegin
mov
First access
mov
xend
else path
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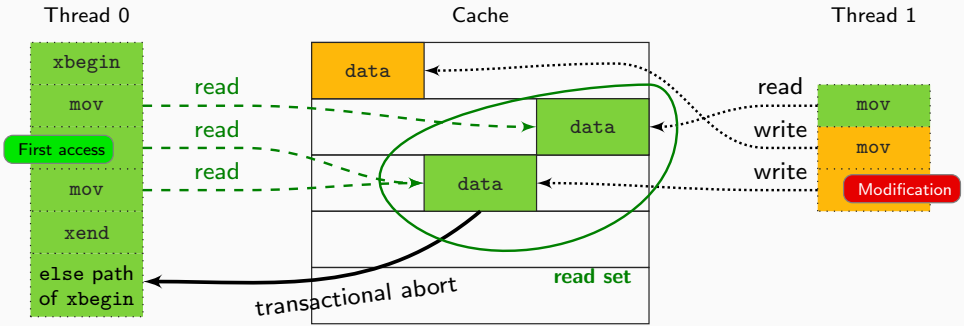
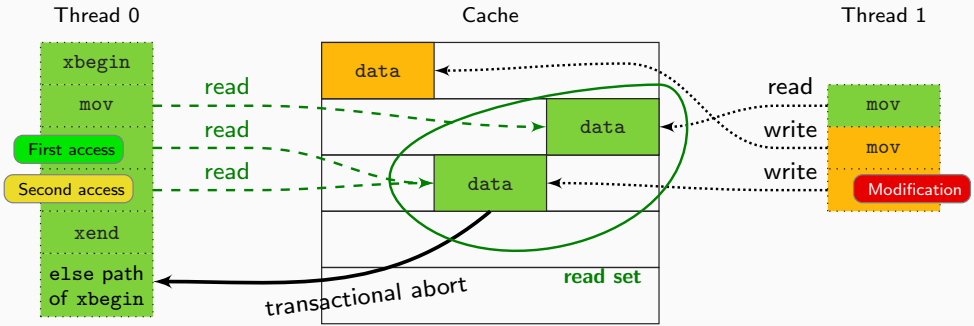
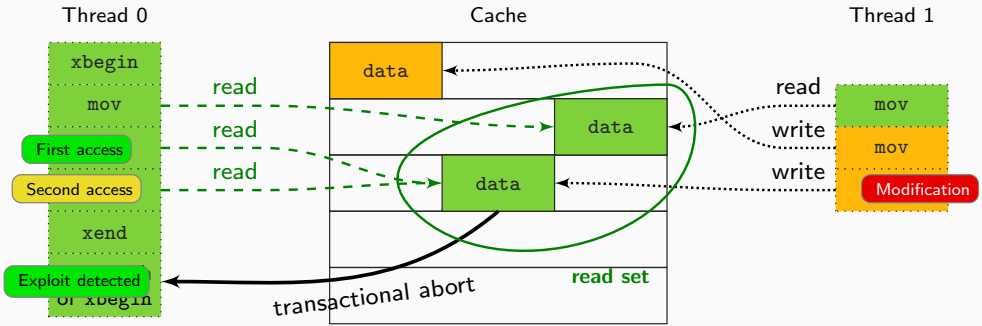
read
read
read
data
data
data
read
write
write
mov
mov
mov
transactional abort
read set


Thread 0
Cache
Thread 1
xbegin
mov
First access
mov
xend
else path
of xbegin
read
read
read
data
data
data
read
write
write
mov
mov
Modification
transactional abort
read set


Thread 0
Cache
Thread 1
xbegin
mov
First access
Second access
xend
else path
of xbegin
read
read
read
data
data
data
read
write
write
mov
mov
Modification
transactional abort
read set


Thread 0
Cache
Thread 1
xbegin
mov
First access
Second access
xend
Exploit detected
or xbegin
read
read
read
data
data
data
read set
transactional abort
read
write
write
mov
mov
Modification

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- Easy to use, 3 additional lines of code are sufficient

```
void play_file(DRMFile* file) {
  doublefetch_t config = doublefetch_init(10);
  doublefetch_start(config);
  if(check_signature(file->header) == ERR_INVALID) {
    // invalid signature
    return;
  }

  int now = get_timestamp_secure();

  if(now < file->header.from || now > file->header.to) {
    // not allowed to watch it now
    return;
  }
  doublefetch_end(config, { printf("Exploit detected!\n"); exit(-1);});

  void* data = decrypt(file->content);
  play_secure(data);
}
```

The Protected Code

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Retry maximum 10 times

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Start protection

Everything in between is atomic

End protection

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- Many CPUs with SGX also have TSX

Conclusion

Black Hat Sound Bytes.

- Side channels can cost you money

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- Side channels can cost you money
- Do not consider side channels out-of-scope

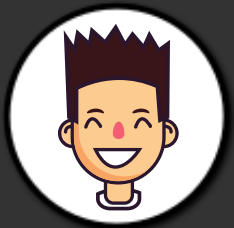
Black Hat Sound Bytes.

- Side channels can cost you money
- Do not consider side channels out-of-scope
- Exploitable code + SGX = exploitable SGX enclave

Thank you!

When Good Turns Evil

Using Intel SGX to Stealthily Steal Bitcoins



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@misc0110

Moritz Lipp
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