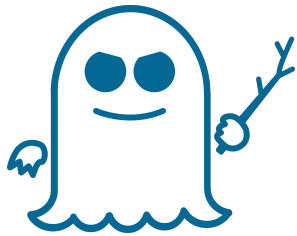
CISPA
HELMHOLTZ CENTER FOR INFORMATION SECURITY

CPU Fuzzing

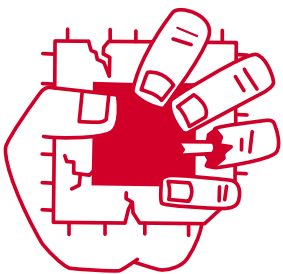
Automatic Discovery of Microarchitectural Attacks

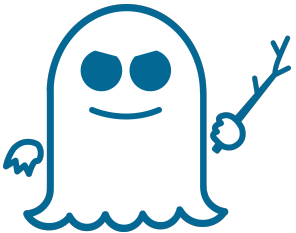
Daniel Weber, Michael Schwarz | May 12, 2023


FIREEYE CYBER
THREAT MAP
DEVELOPING STORY
COMPUTER CHIP FLAWS IMPACT BILLIONS OF DEVICES
LIVE
CNN
DAX ▲164.69
NEWS STREAM



Daniel Weber (@weber_daniel), Michael Schwarz (@misc0110)





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Microarchitectural

attacks

Microarchitectural attacks

How do they **work**?

Microarchitectural attacks

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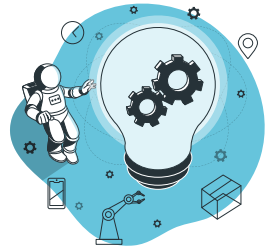

How can we find them **efficiently**?

Who am I?

Daniel Weber

PhD Student @ CISPA Helmholtz Center for Information Security

Research on CPU Security and Side Channels

@weber_daniel

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Who am I?

Michael Schwarz

Faculty @ CISPA Helmholtz Center for Information Security

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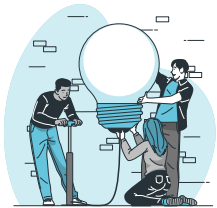
@misc0110

michael.schwarz@cispa.de

Team



Osiris Research Team

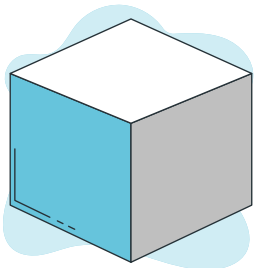
Daniel Weber, *Ahmad Ibrahim, Hamed Nemati,* ***Michael Schwarz***, *Christian Rossow*

Transynther Research Team

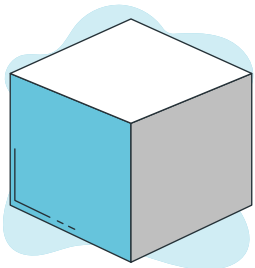
Daniel Moghimi, Moritz Lipp, Berk Sunar, ***Michael Schwarz***

MSRevelio Research Team

Andreas Kogler, ***Daniel Weber***, *Martin Haubenwallner, Moritz Lipp, Daniel Gruss,* ***Michael Schwarz***

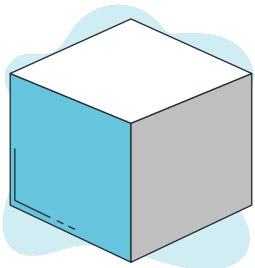


CPU



CPU

Specification (ISA)



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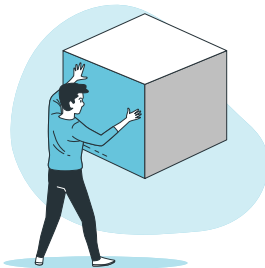


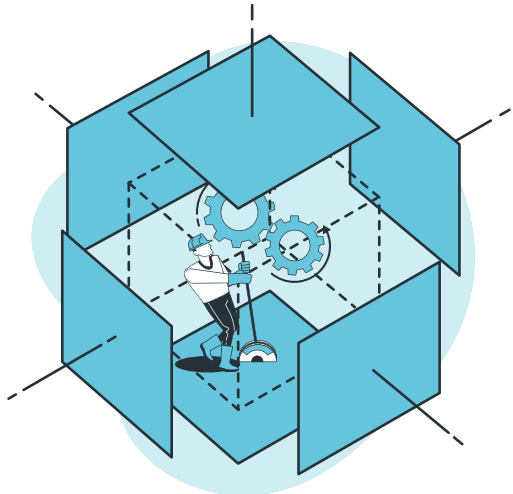
Interaction

Everything **works**
as expected

Everything **works**
as expected

No bugs

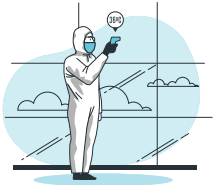
How can you attack this?



Information **leaks** through **side effects**

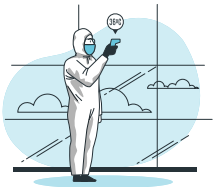
Power Consumption

Power Consumption



Temperature

Power Consumption



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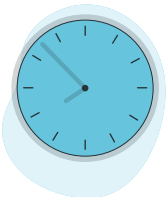
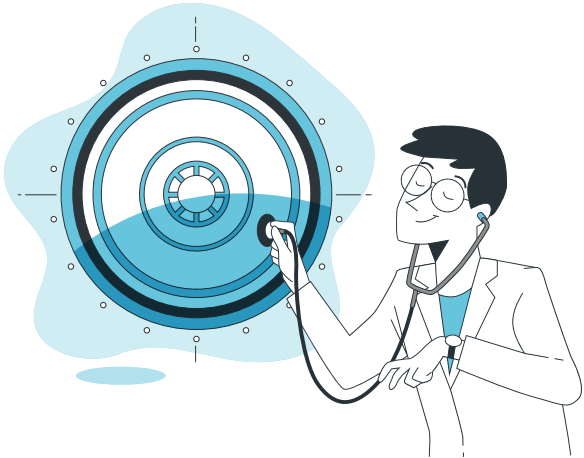
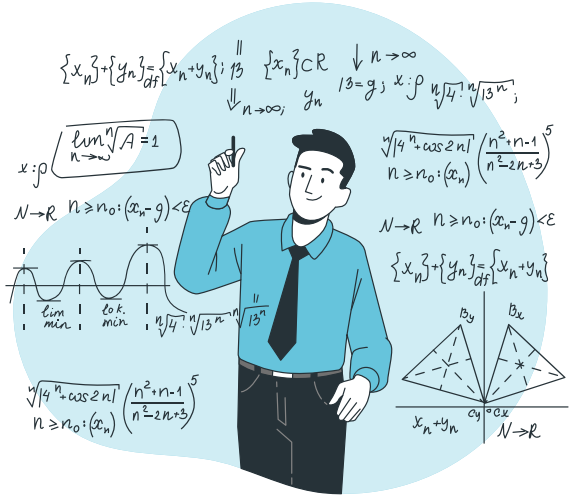


Execution Time



Observe Device

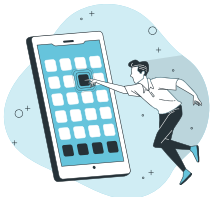


Evaluate data

Get the secrets. **Easy as that!**

Reality **is not** as easy

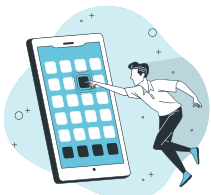
Properties



Software-only

No Physical Access required

Properties



Software-only

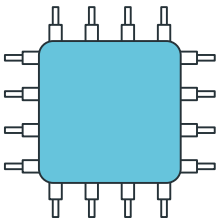
No Physical Access required

Understand Inner Workings

of the CPU

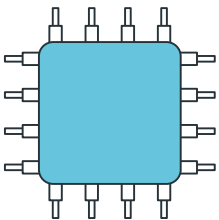
What can we observe? How does a CPU work internally?

Architecture vs Microarchitecture



- Instruction Set Architecture (ISA) is an **abstract model** of a computer (x86, ARMv8, SPARC, …)

Architecture vs Microarchitecture



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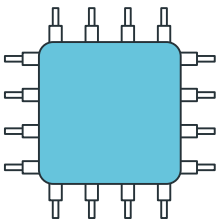
- **Interface** between hardware and software

Architecture vs Microarchitecture



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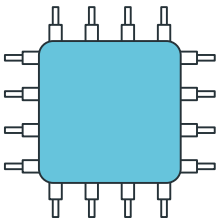
- Microarchitecture is an ISA **implementation**

Architecture vs Microarchitecture



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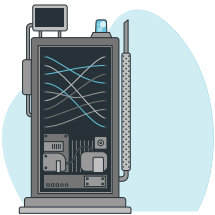
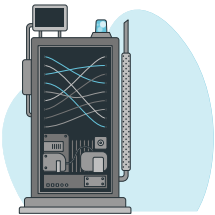
Optimizations



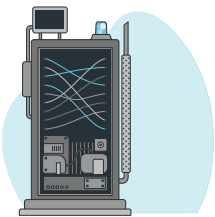
- Modern CPUs contain multiple **microarchitectural elements**

Optimizations



- Modern CPUs contain multiple **microarchitectural elements**
- **Transparent** for the programmer

Optimizations

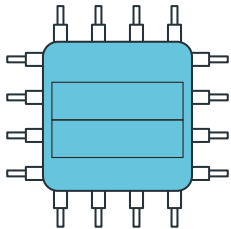


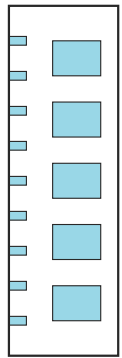
- Modern CPUs contain multiple **microarchitectural elements**
- **Transparent** for the programmer
- **Optimize** for performance, power consumption, …

CPU Optimization: Cache

```
printf("%d", i);

printf("%d", i);
```





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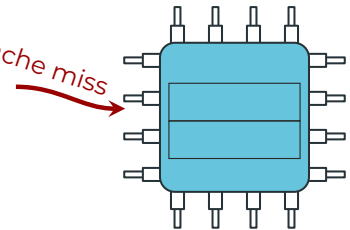

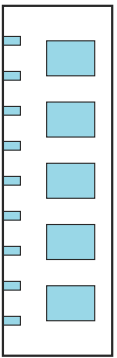

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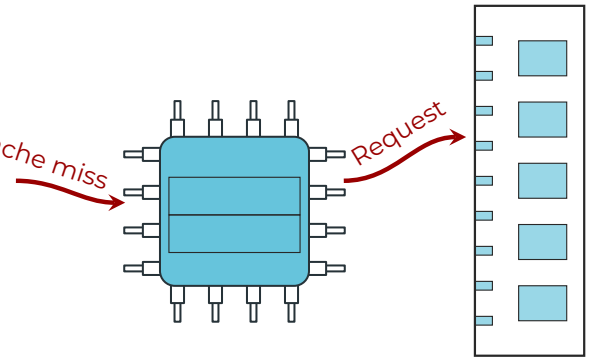

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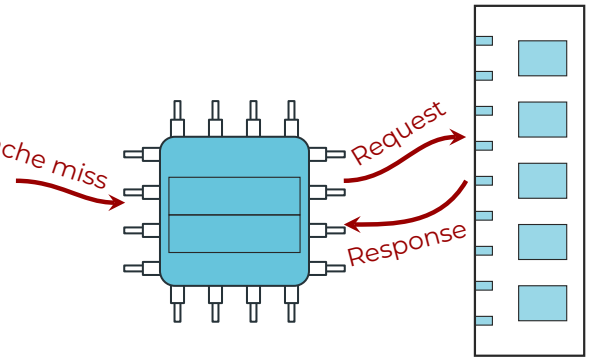

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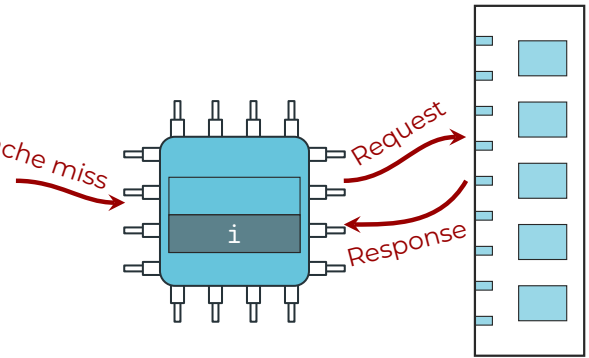

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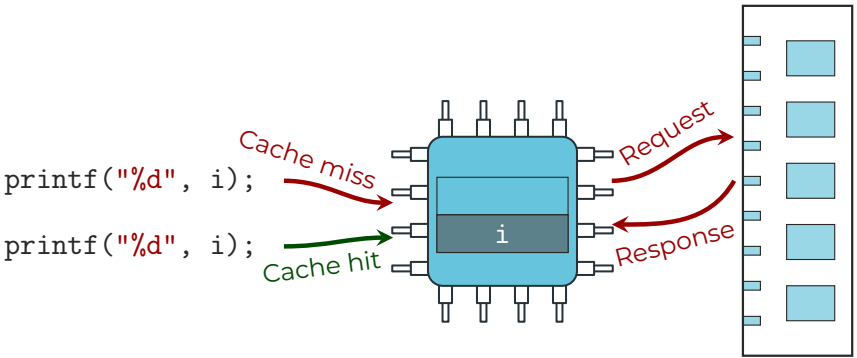

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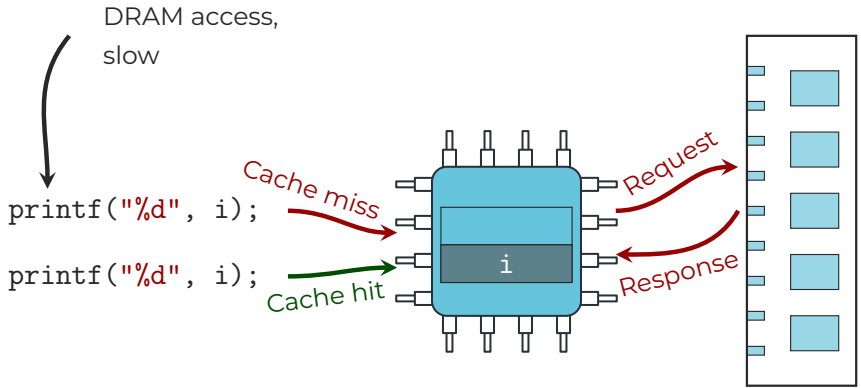
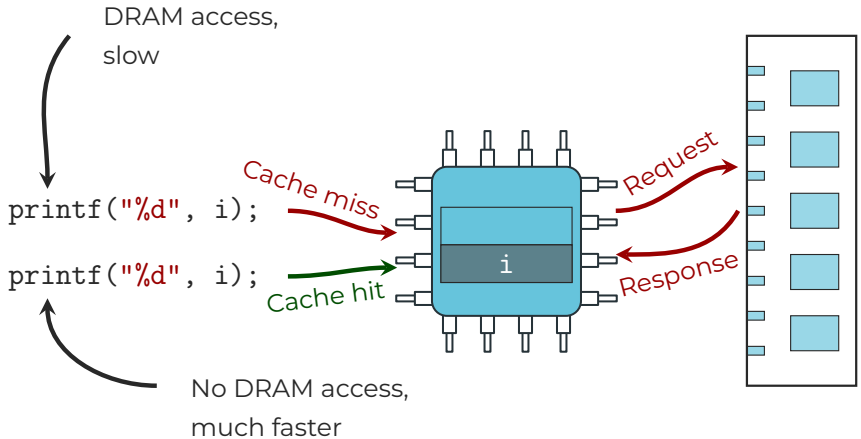
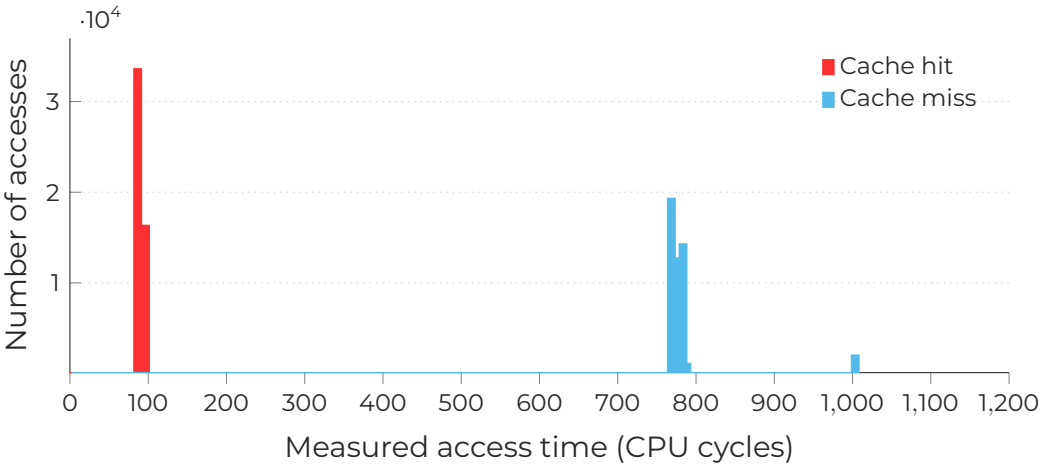


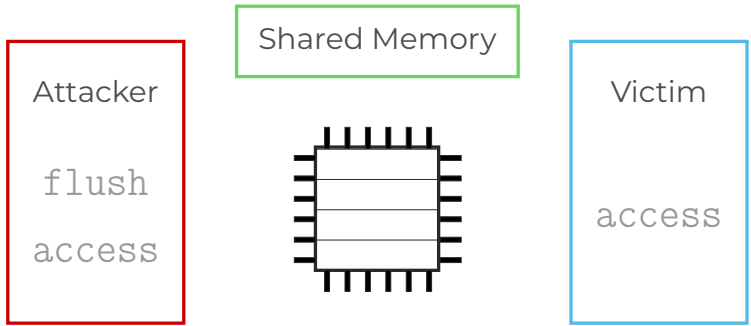
CPU Optimization: Cache



Caching speeds up Memory Accesses



Flush+Reload



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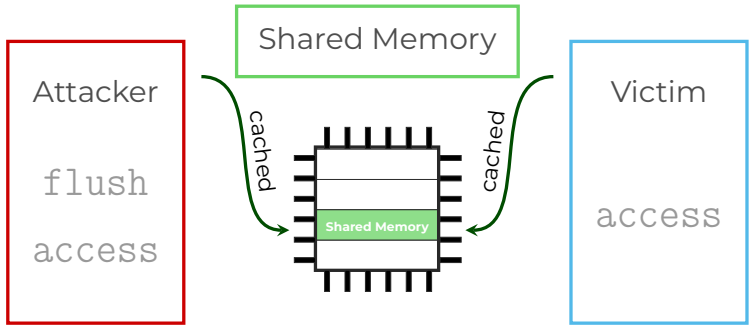

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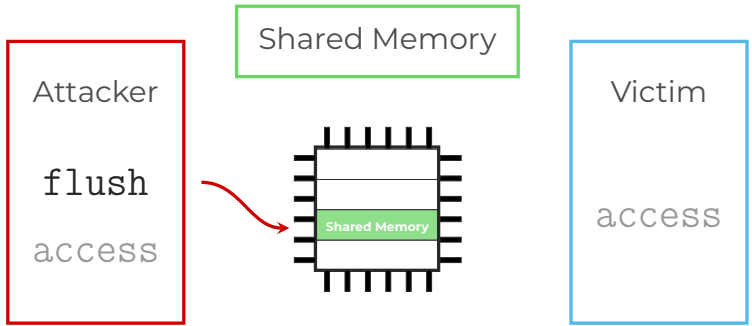

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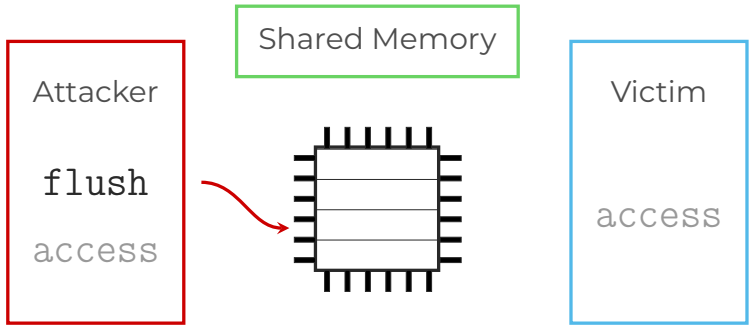

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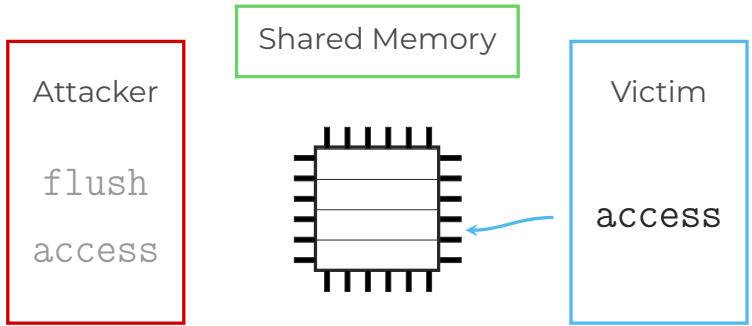

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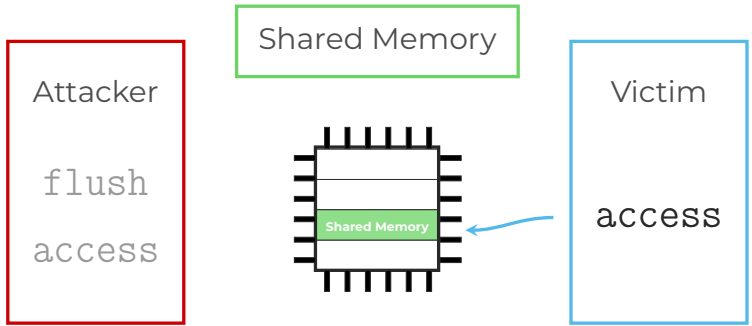

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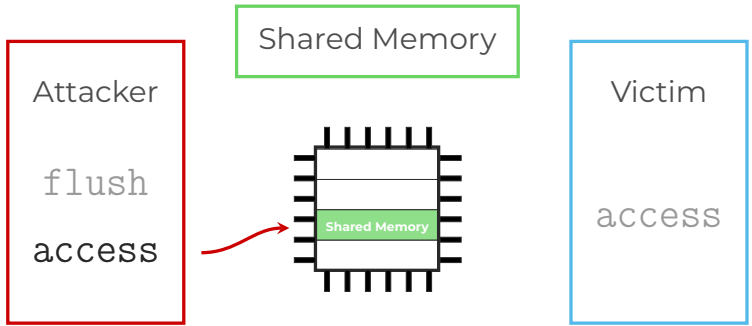

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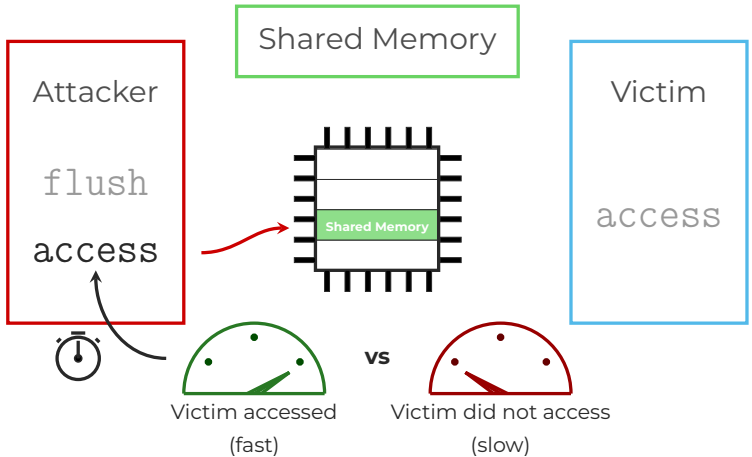

Cache Attacks

- Leak **cryptographic keys**

Cache Attacks

- Leak **cryptographic keys**
- Leak information on **co-located virtual machines**

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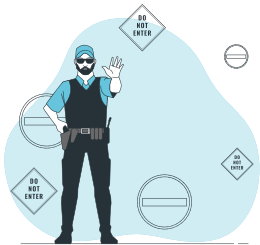
- **Monitor** function calls of other applications

Cache Attacks

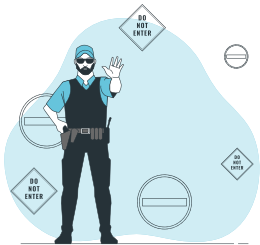
- Leak **cryptographic keys**
- Leak information on **co-located virtual machines**
- **Monitor** function calls of other applications
- Build **covert communication channels**
- …

Motivation



Leakage of **1-2** Instructions

Motivation



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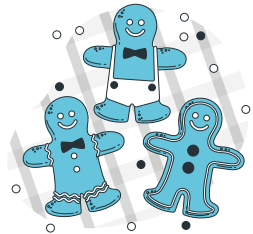
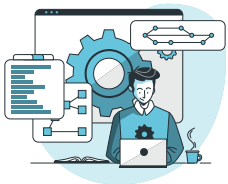


There are **>3000** instructions

How do you find **these** attacks?

Read documentation and patents

Read documentation and patents



Develop ideas

Read documentation and patents

Develop ideas

Test ideas and start over

New CPU, **New** Features

New CPU, **New** Features

Repeat from the beginning

Finding side channels and vulnerabilities is a **complex** and **time-consuming** process

Can we do **better**?

Automation for Side-Channel Search

- How can you find bugs in **software** in an automated way?

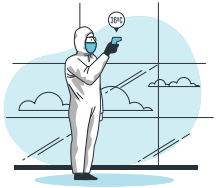
Automation for Side-Channel Search

- How can you find bugs in **software** in an automated way?
- **Fuzzing** is an automated software testing method
  - Inject invalid, malformed, unexpected input to a program

Automation for Side-Channel Search

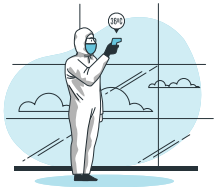
- How can you find bugs in **software** in an automated way?
- **Fuzzing** is an automated software testing method
  - Inject invalid, malformed, unexpected input to a program
- Can we **apply a similar approach** do find microarchitectural side-channels?

Challenges when Fuzzing CPUs



Limited Feedback

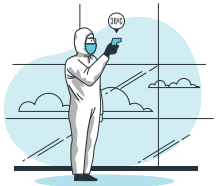
Challenges when Fuzzing CPUs



Limited Feedback

Dirty States

Challenges when Fuzzing CPUs



Limited Feedback

Dirty States

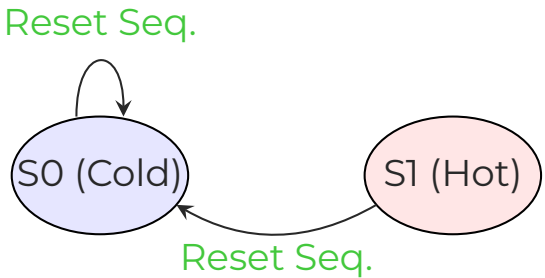
System Noise

Side Channel Search

Can we **automatically decide** whether we **found a side channel?**

Modelling Side Channels

Modelling Side Channels



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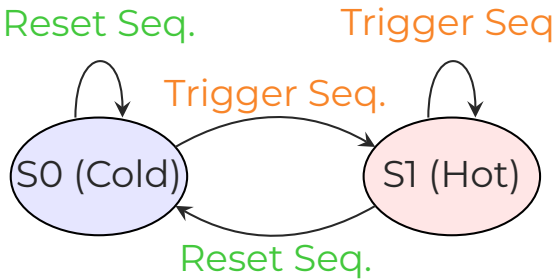

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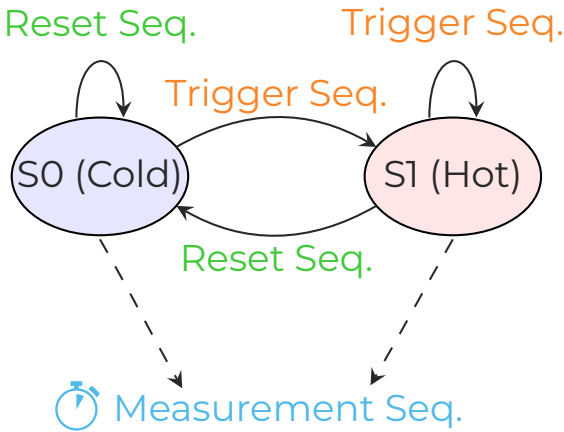

Testing Potential Side Channels

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Cold path S0

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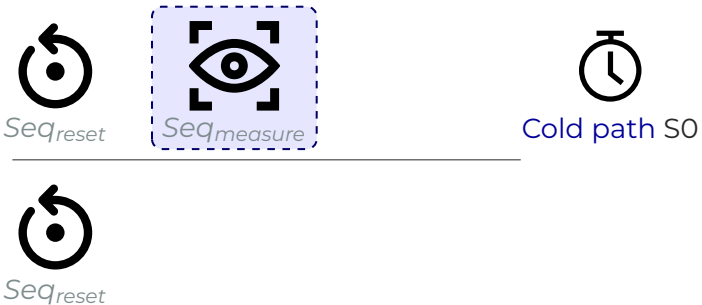

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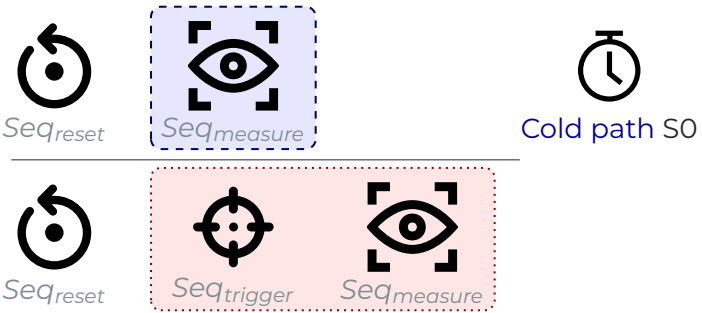

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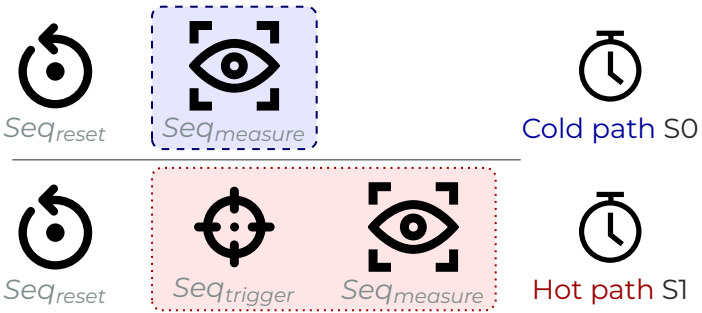

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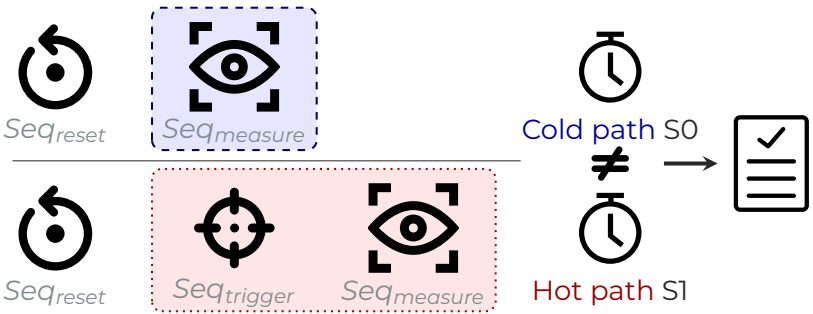

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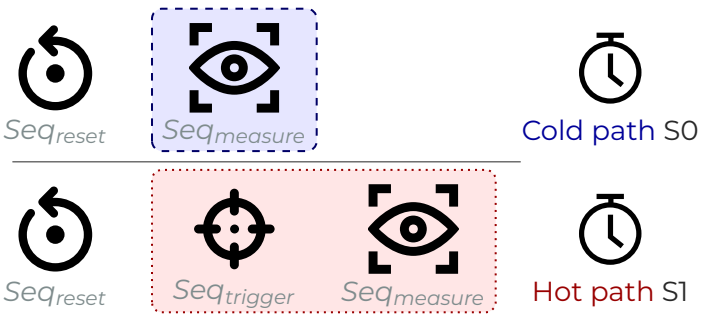

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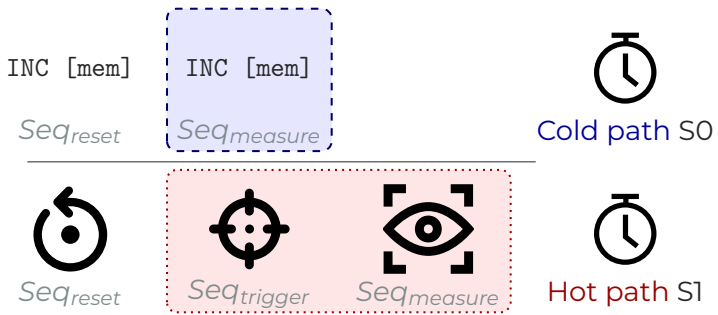

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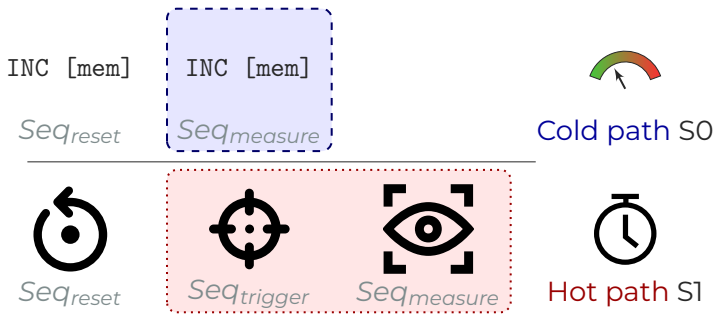

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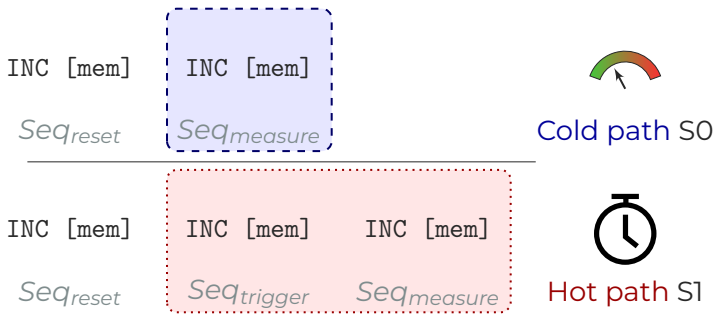

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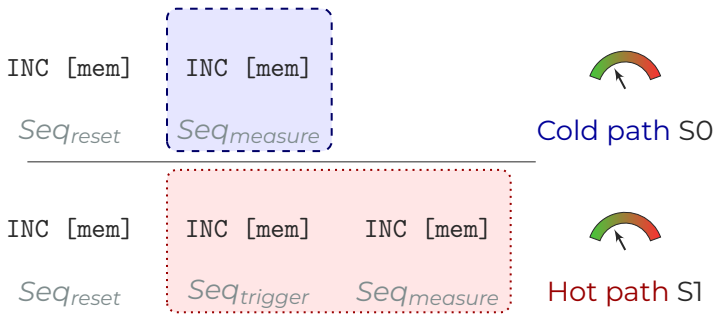

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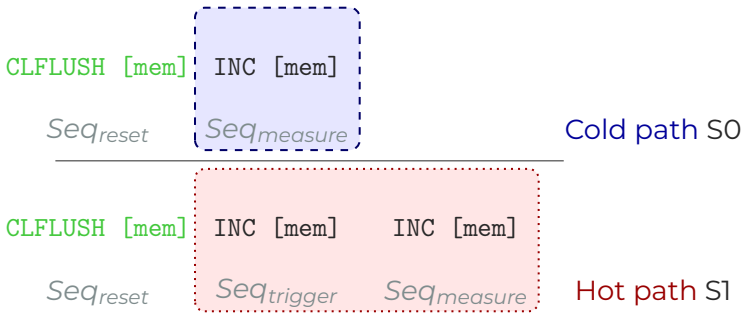

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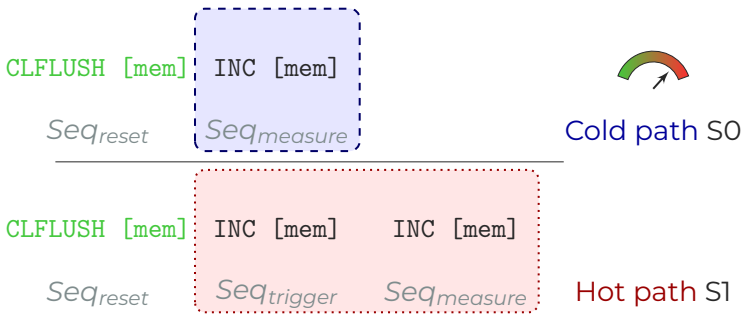

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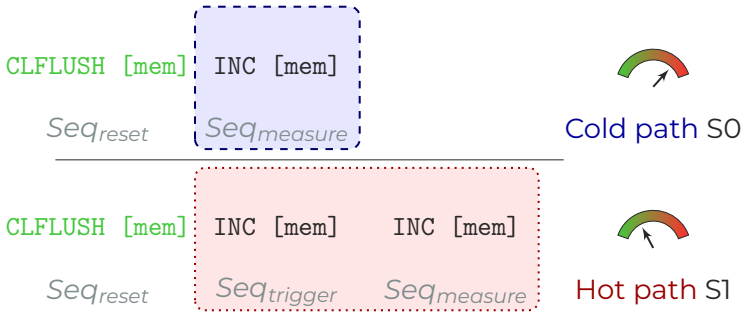

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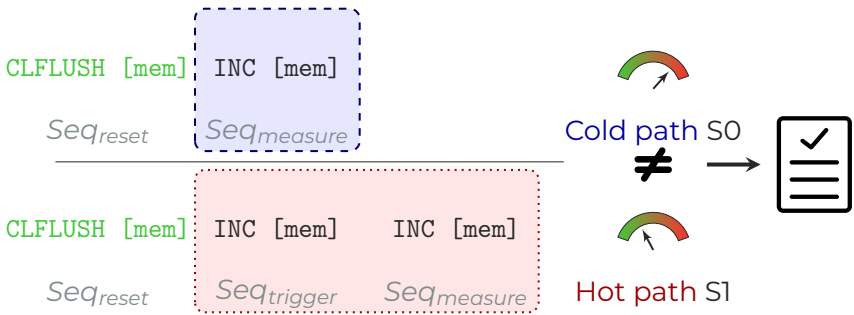
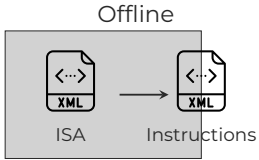


Let’s Fuzz for Side Channels

Osiris – Fuzzing x86 CPUs for Side Channels



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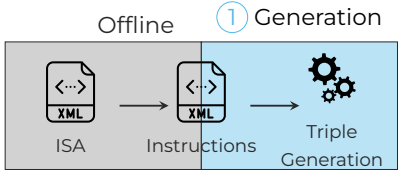

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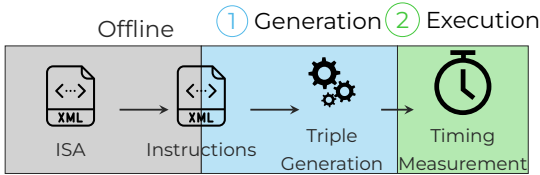

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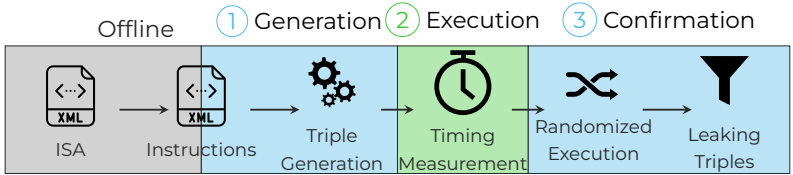

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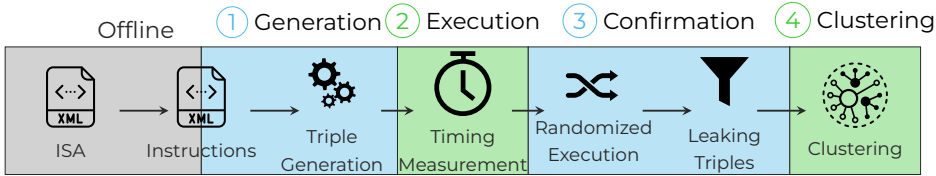

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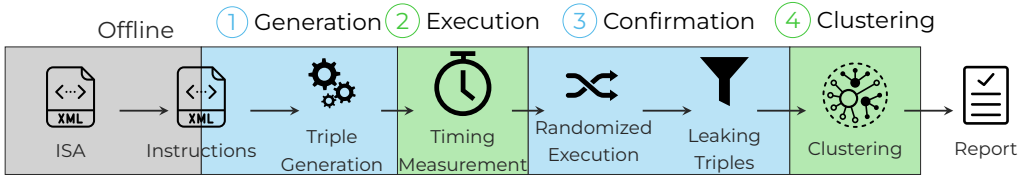

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4 days

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2 side channels reproduced

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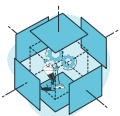

4 new side channels

Osiris – Results Overview

4 days

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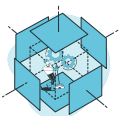

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1 new attack

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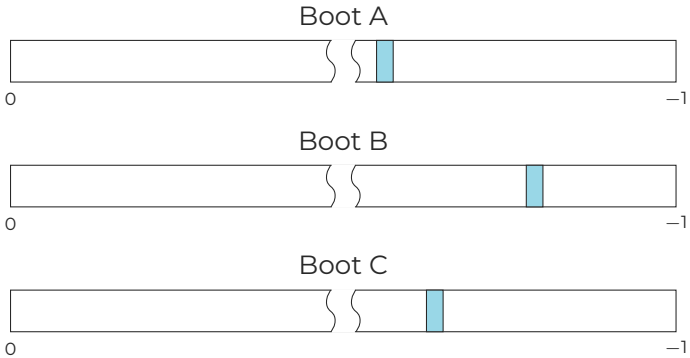
- OS Kernels are **protected by KASLR**
- Memory location of the kernel is **randomized**
- Attacker **do not know where** to attack

KASLR: Kernel Address Space Layout Randomization



- Kernel is loaded to a different offset on every boot

Findings – FlushConflict

- **KASLR break** based on MOVNT and transient execution

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- Breaks KASLR reliably in **136ms (average)**

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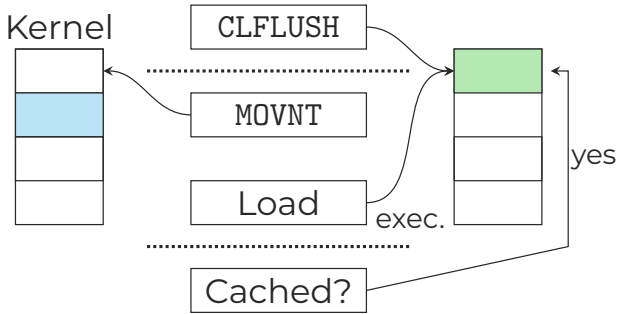

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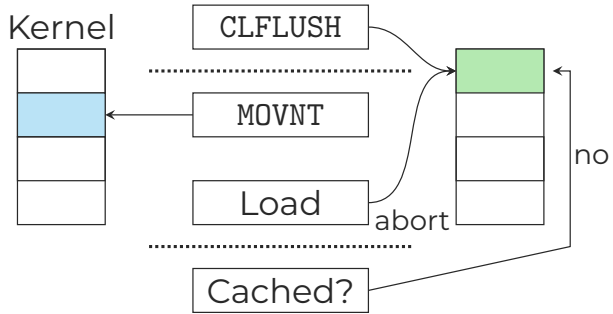

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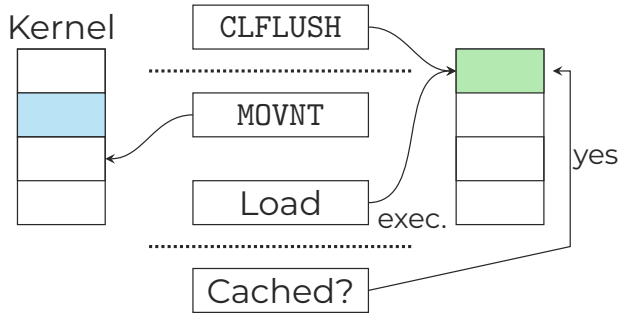

FlushConflict Live Demo

Osiris – Lessons Learned

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→ Osiris prototype is currently limited to 1 instruction per sequence

Can we find **more powerful attacks?**

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Can we **leak actual data** instead of meta data?

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- With **Meltdown**, we exploit out-of-order execution to leak the content of **inaccessible** kernel addresses

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  - → Faulty state is never architecturally visible
  - → Use a side-channel (Flush+Reload) to make it visible
- Many different attack variants:
  - → Fallout, ZombieLoad, CrossTalk, …

Meltdown-type Attacks

User Memory

	A	B
C	D	E
F	G	H
I	J	K
L	M	N
O	P	Q
R	S	T
U	V	W
X	Y	Z

```
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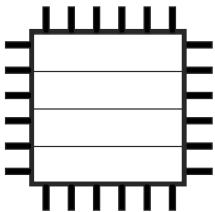

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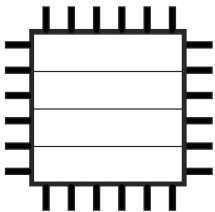

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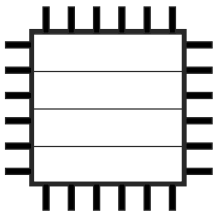
Fault

Out of order

```
mem[value]
```

K



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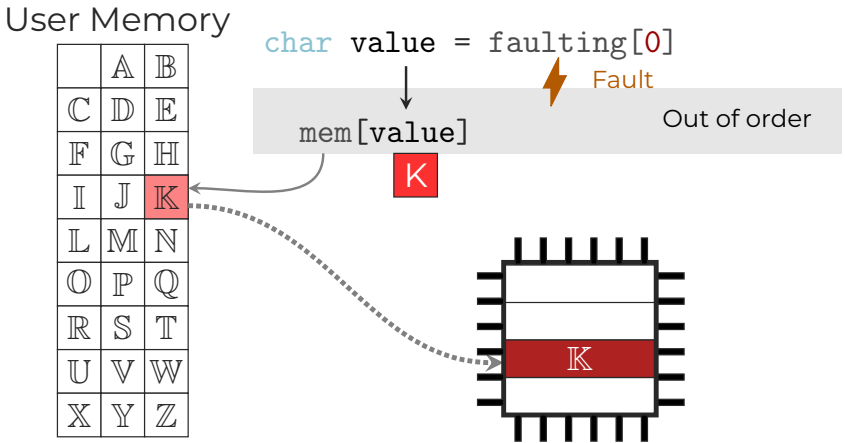

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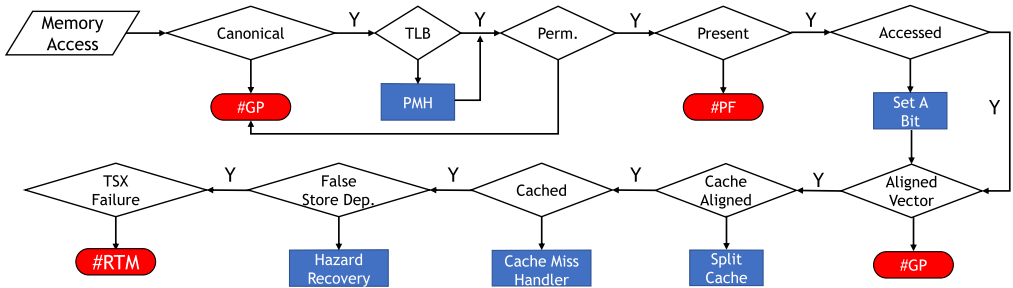
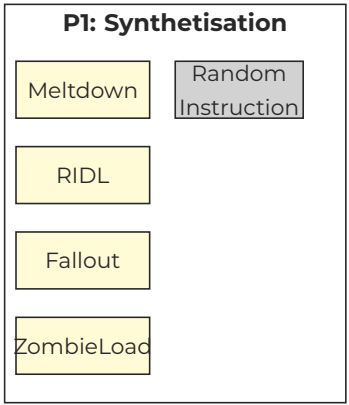


Fuzzing for Meltdown-type Attacks

Transynther – Fuzzing for Meltdown-type Attacks



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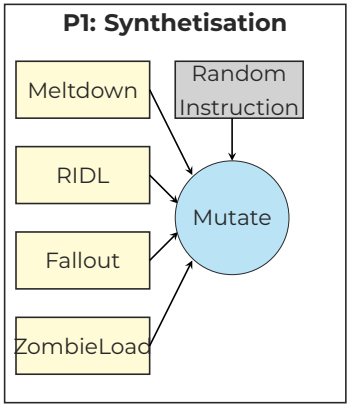

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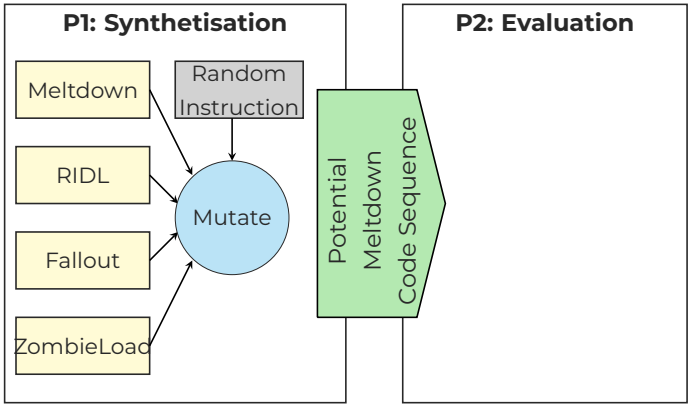

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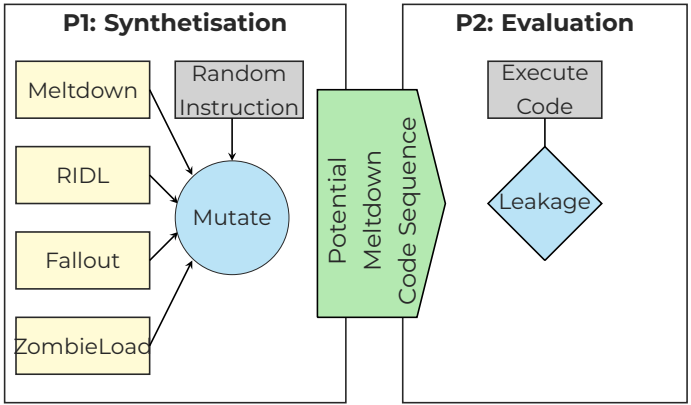

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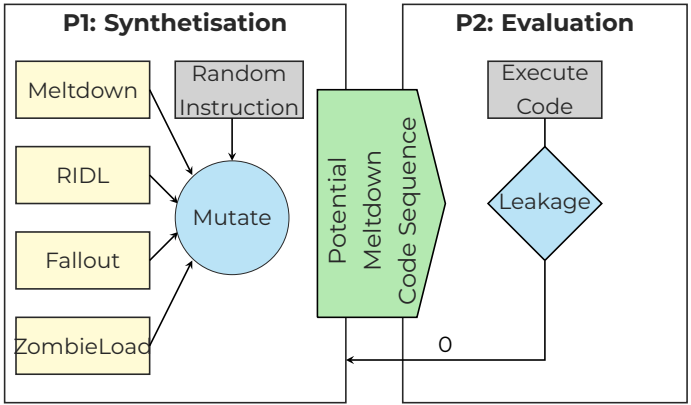

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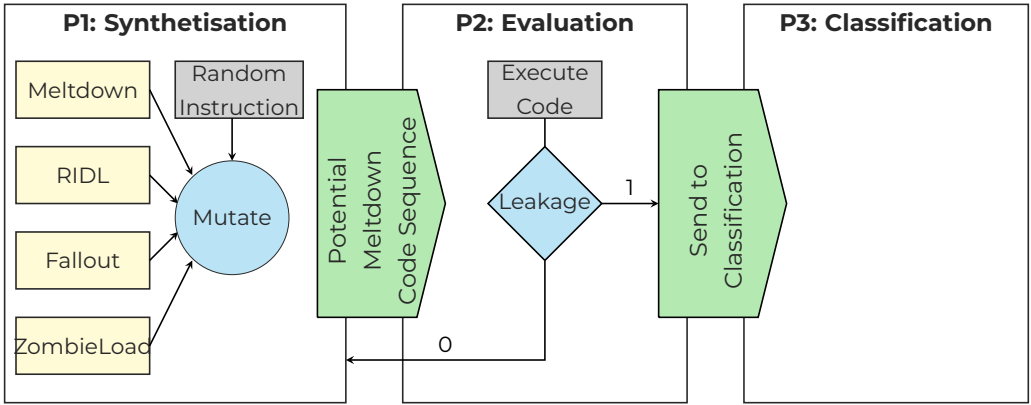

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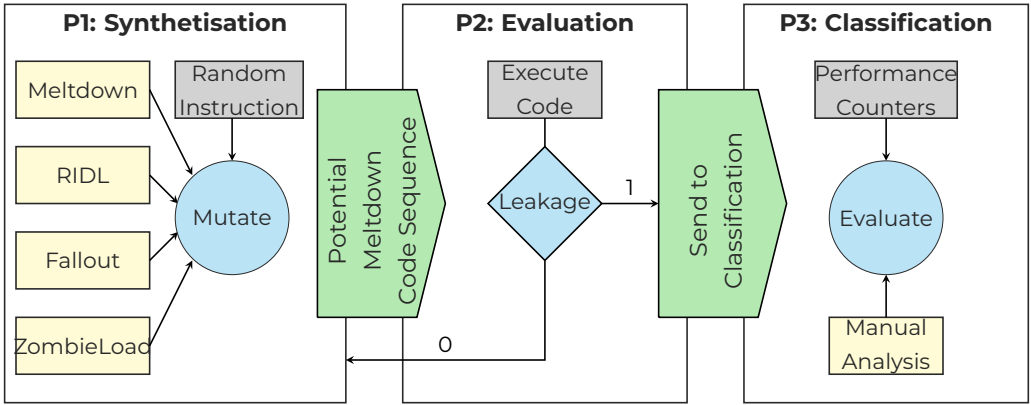

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Findings – Reenabling MDS Attack

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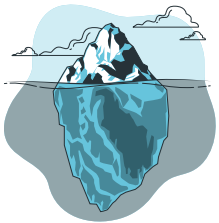
→ Leaked RSA key while decoding in OpenSSL

Findings – MDS Attack on Ice Lake



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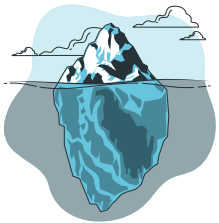

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→ Transynther found a working MDS attack

  - Variant of a Fallout attack

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- **Post-analysis** can also be automated
- **Regression bugs can be found** using automated tools

Are there also **architectural bugs**?

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What about **unknown instructions**?

Finding Unknown Instructions

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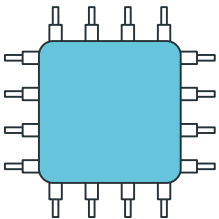
Finding Unknown Instructions

- **Sandsifter**[a] searches for undocumented x86 instructions
  - Trick to check for valid instruction bytes using page faults
- **Haruspex**[b] uses speculative execution and performance counters

[a] Sandsifter (Christopher Domas): `https://github.com/xoreaxeaxeax/sandsifter`
[b] Haruspex (Can Bölük): `https://github.com/can1357/haruspex`

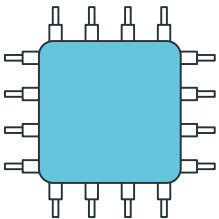
What else is **left**?

Model-Specific Registers and their Hidden Secrets



- Model-Specific Registers (MSRs) are **special CPU control registers**

Model-Specific Registers and their Hidden Secrets

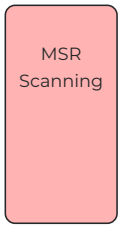


- Model-Specific Registers (MSRs) are **special CPU control registers**
- VIA C3 CPU had backdoor access[a] hidden behind an **undocumented MSR bit**

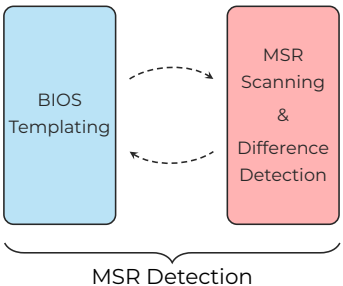
[a] GOD MODE unlocked: Hardware backdoors in x86 CPUs (Christopher Domas – BlackHat USA '18)

Searching for Undocumented MSRs

MSRevelio – Overview



MSRevelio – Overview



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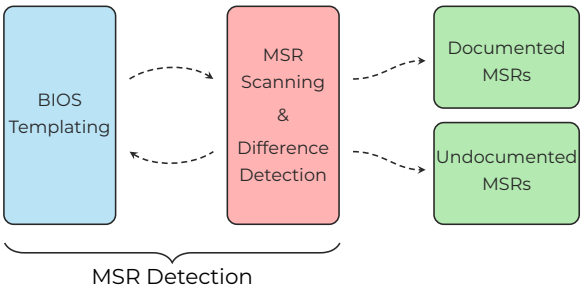

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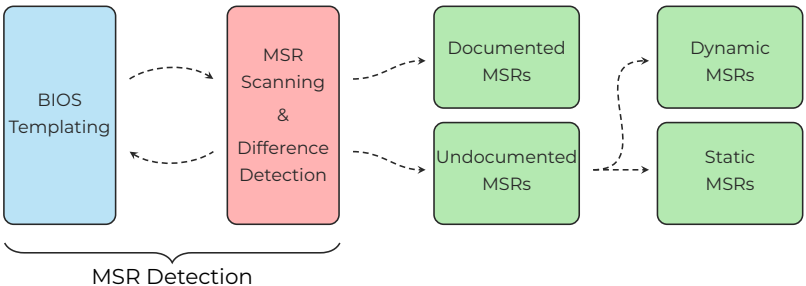

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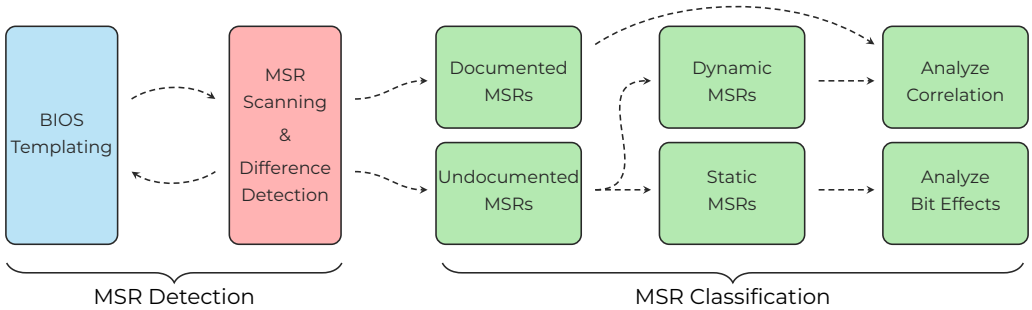

MSRevelio – Results Overview

5890 undocumented MSRs

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New MSRs hint towards vulnerabilities

Findings – Undisclosed Attacks

- MSRs often used to introduce **vulnerability fixes**

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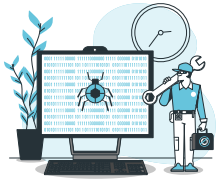
- MSRs exist **before public disclosure**

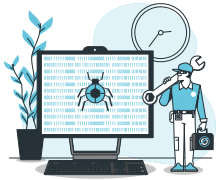
→ Useful for 1-Day Exploits

Findings – Attack Mitigation



- Mitigate **prefetch side-channel attacks**

Findings – Attack Mitigation



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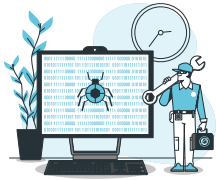

- Mitigate **prefetch side-channel attacks**
- Reduce **Crosstalk leakage**
- Reduce **Medusa leakage**

MSRevelio – Lessons Learned

- Searching for **unknown behavior is hard**

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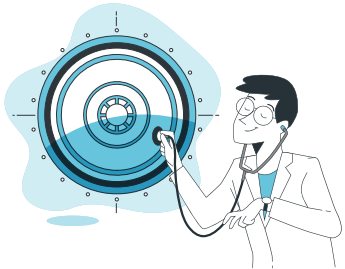
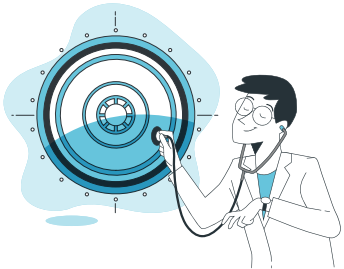
- Automation allows **tracing changes between releases**
  (cf. Transynther)

Conclusion



Automated
side-channel discovery



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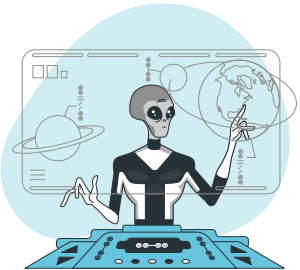

Automated
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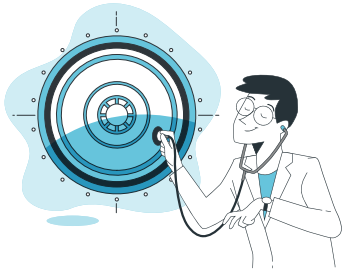

Automated
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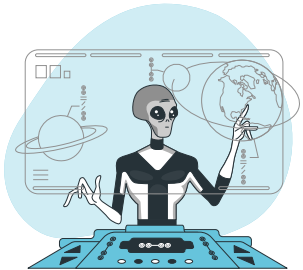

Automated
transient-execution attack discovery

Automated detection of
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CPU Fuzzing – Lessons Learned

- **Scalability**: Automation is easier than manual efforts (even if limited)

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- **Versatile**: Execute on various microarchitectures

Open-Source – Feel Free to Test

All our tools are **accessible** and **open source**:

Open-Source – Feel Free to Test

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→ `https://github.com/D4nielMoghimi/medusa`

→ `https://github.com/CISPA/osiris`

→ `https://github.com/IAIK/msrevelio`

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  - **regression** testing
  - **extensible** for new building blocks and architectures
- Despite **limitations**, great toolkit and support for manual efforts
- Play an **essential role** in CPU research

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CPU Fuzzing

Automatic Discovery of Microarchitectural Attacks

Daniel Weber, Michael Schwarz | May 12, 2023

References

- Slides partially by Moritz Lipp
- Icons and Images from `storyset.com`
- Images from CNN