

Are Microarchitectural Attacks still possible on Flawless Hardware?

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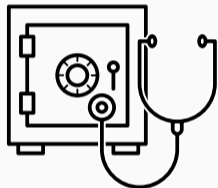
 @ekraft95

 erik.kraft@student.tugraz.at

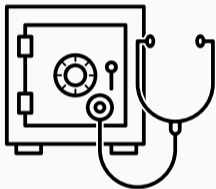


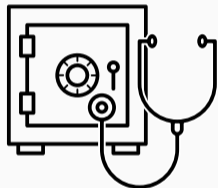
- Daniel Gruss (Graz University of Technology)
- Trishita Tiwari (Boston University)
- Ari Trachtenberg (Boston University)
- Jason Hennessey (NetApp)
- Alex Ionescu (CrowdStrike)
- Anders Fogh (Intel)

- Bug-free software does not mean safe execution



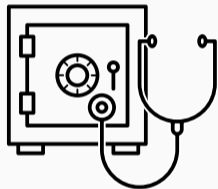
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Power consumption

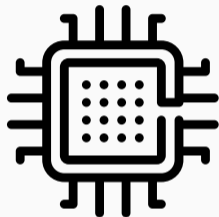


Execution time

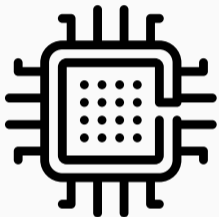


CPU caches

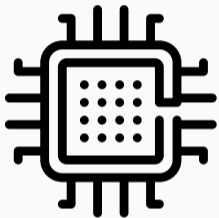




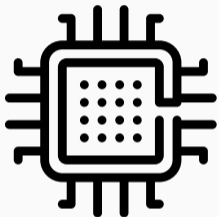
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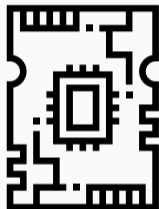


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- Microarchitecture is an ISA **implementation**



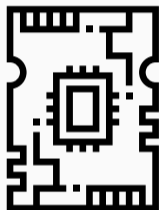
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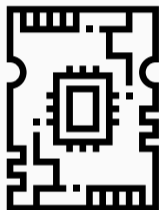
Caches and buffers



Predictors



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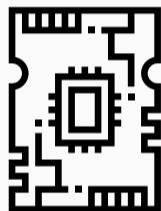
Caches and buffers



Predictors



- **Transparent** for the programmer



- Modern CPUs contain multiple **microarchitectural elements**



Caches and buffers

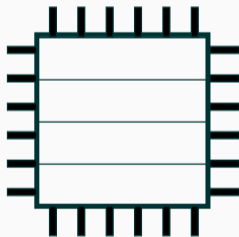


Predictors



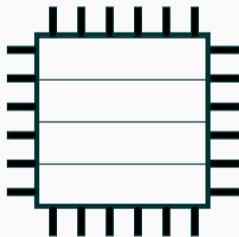
- **Transparent** for the programmer
- Timing optimizations → side-channel leakage

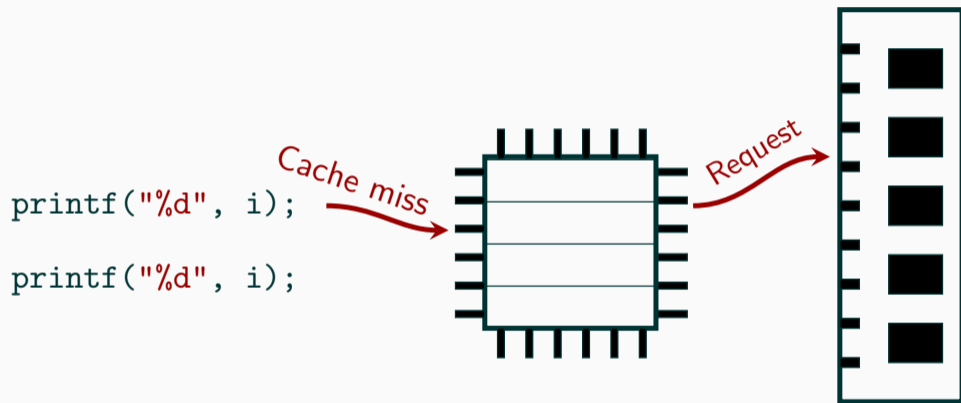

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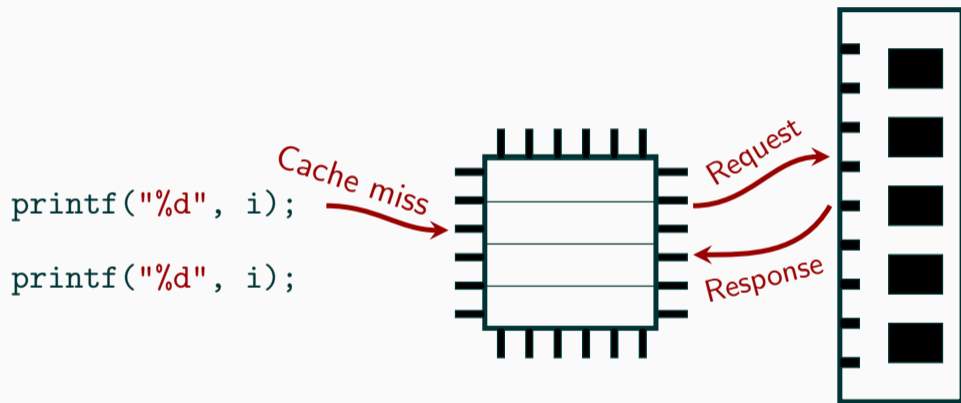


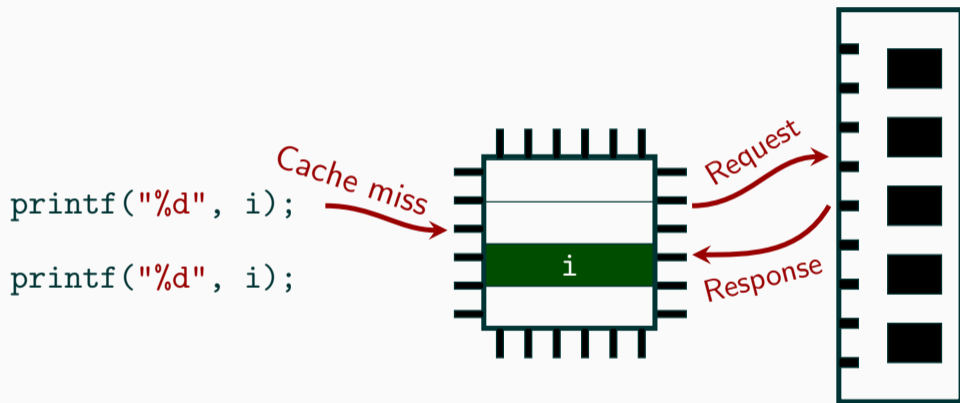
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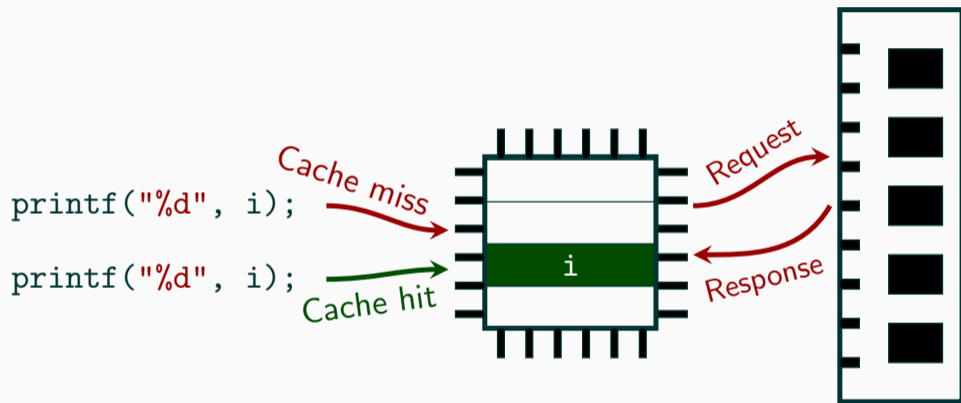
Cache miss

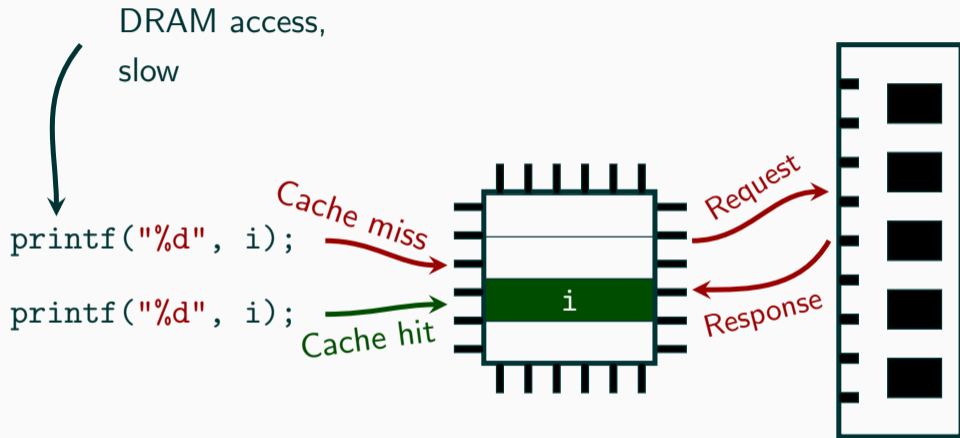


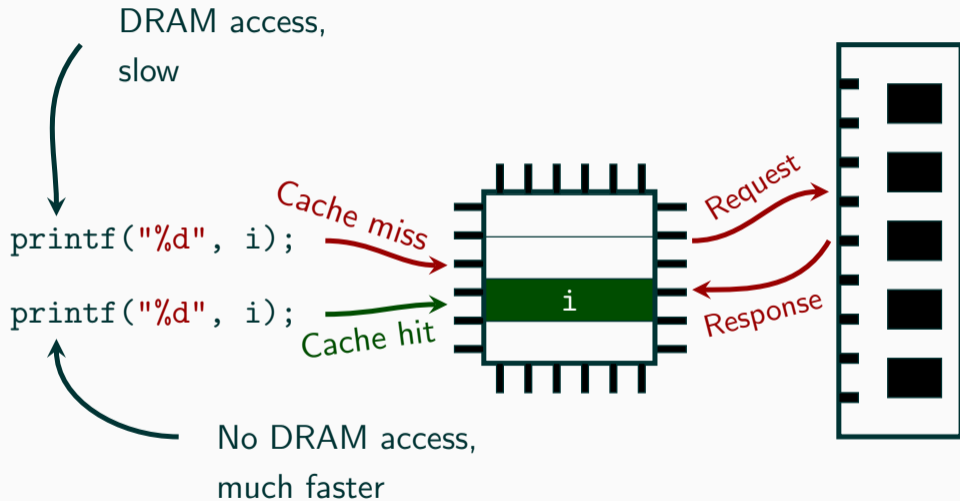


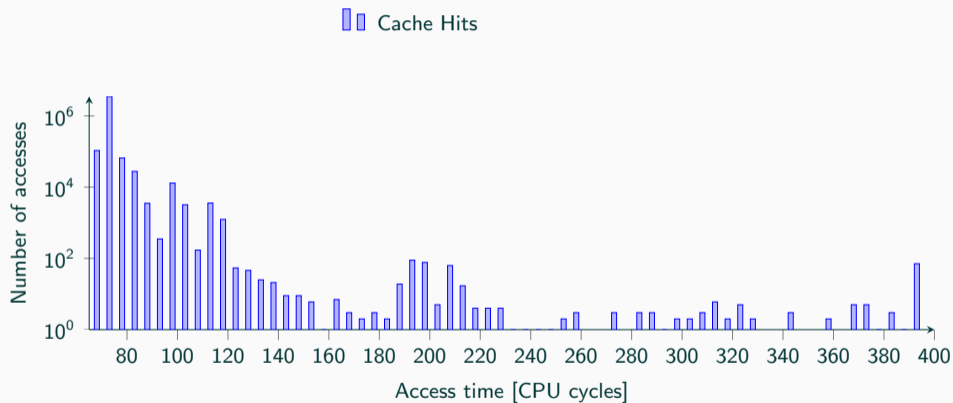


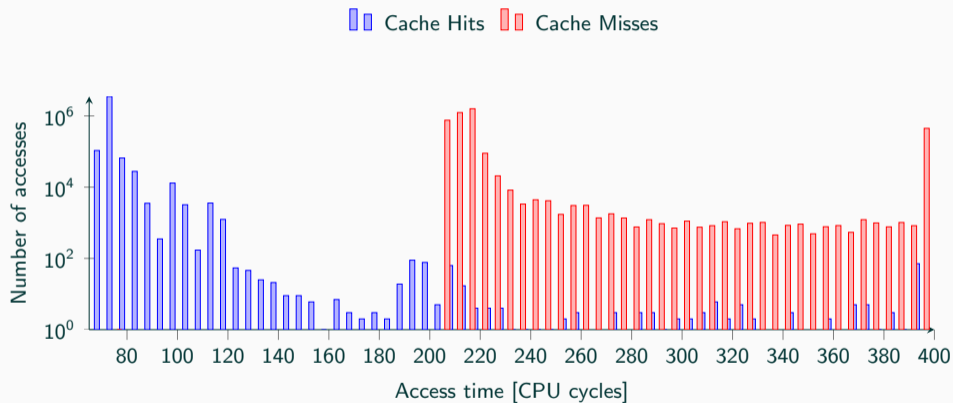


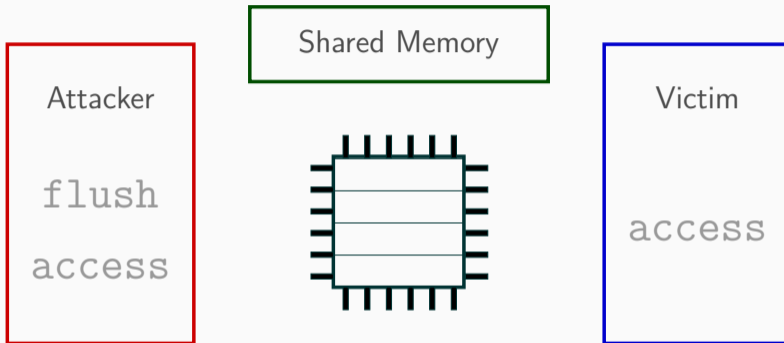


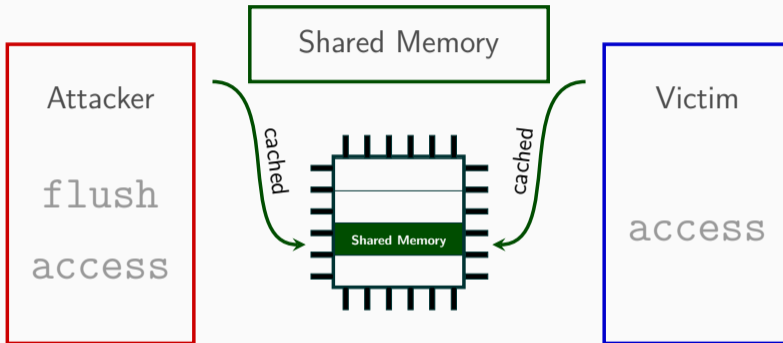


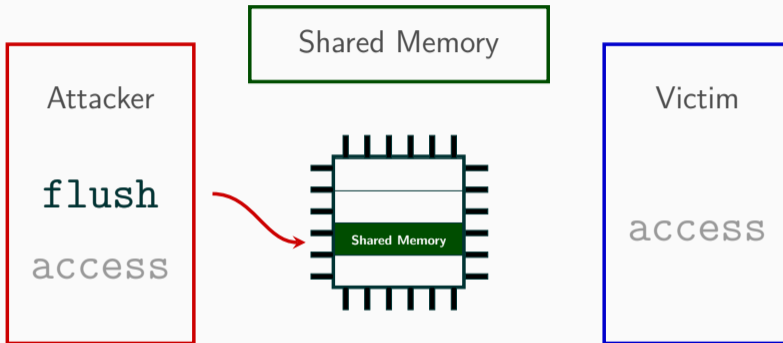


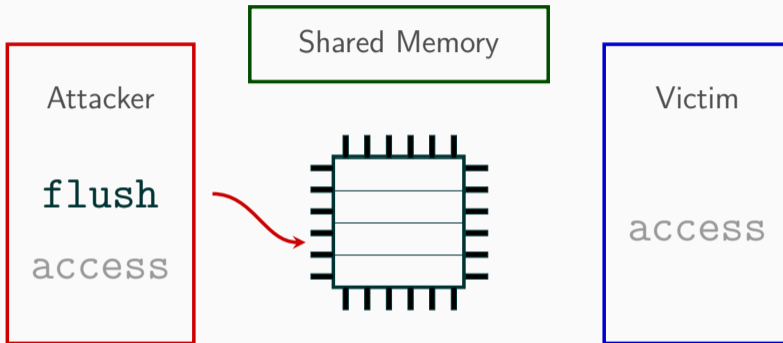


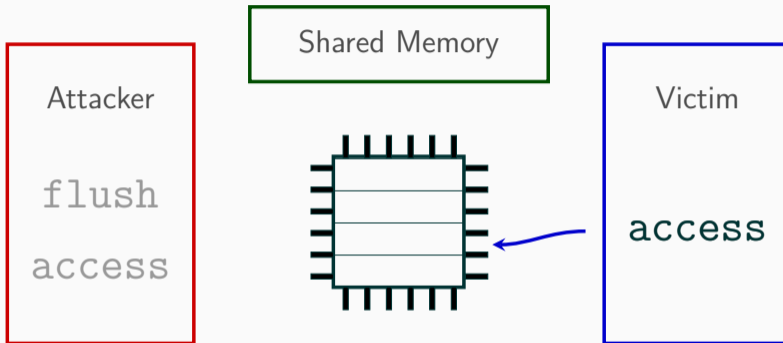


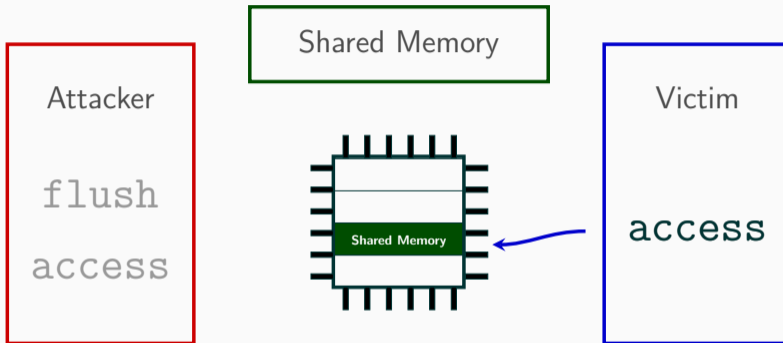


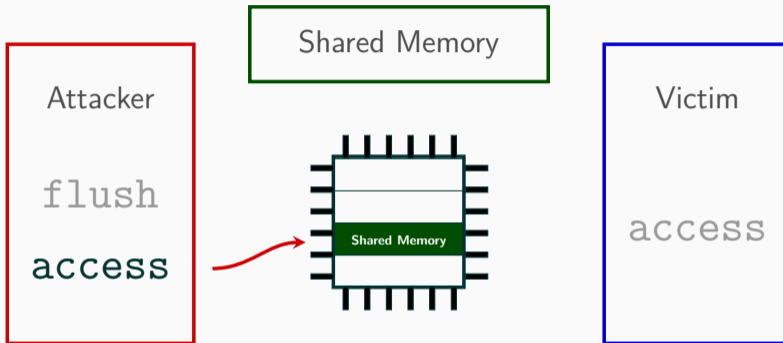


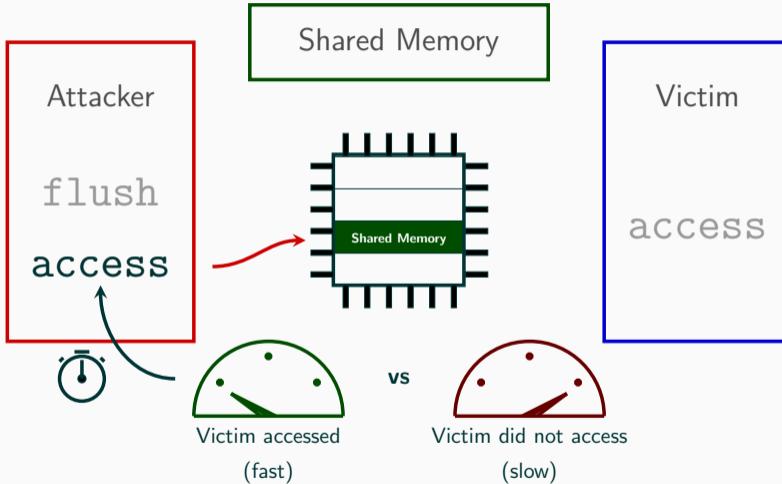


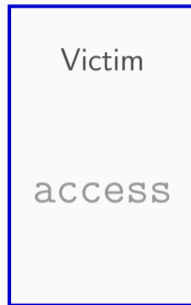
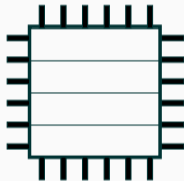


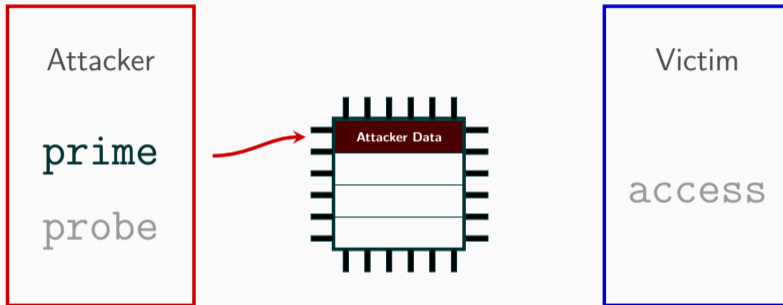


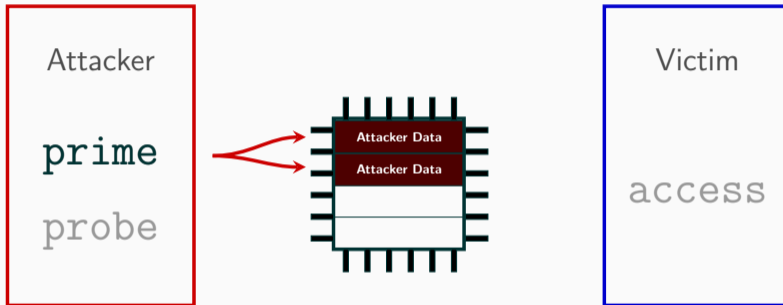


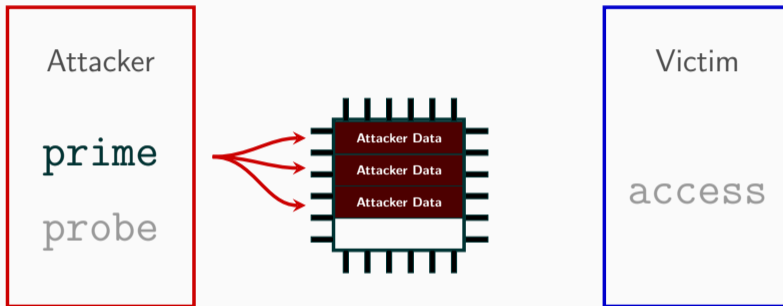


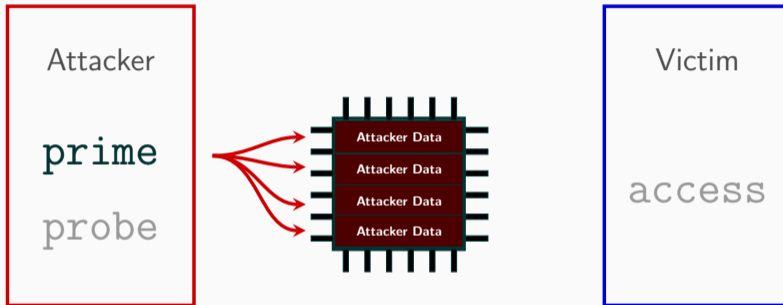


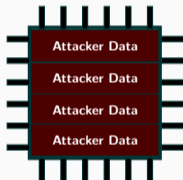


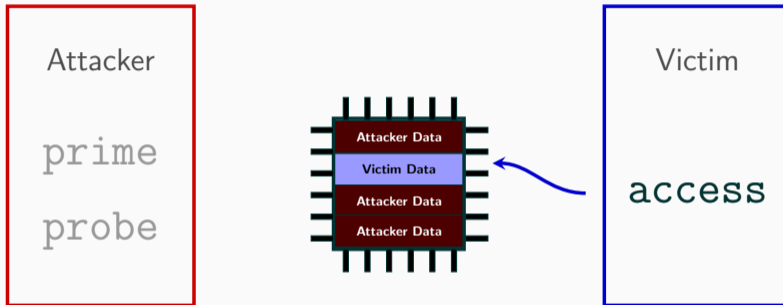


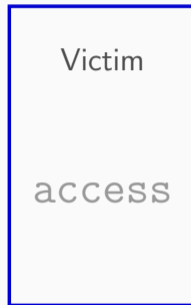
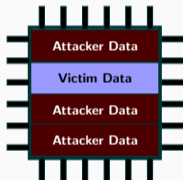


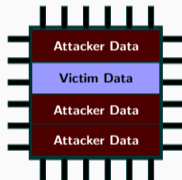


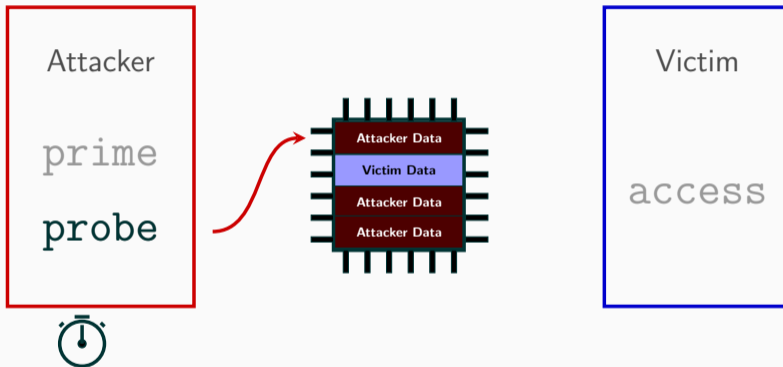


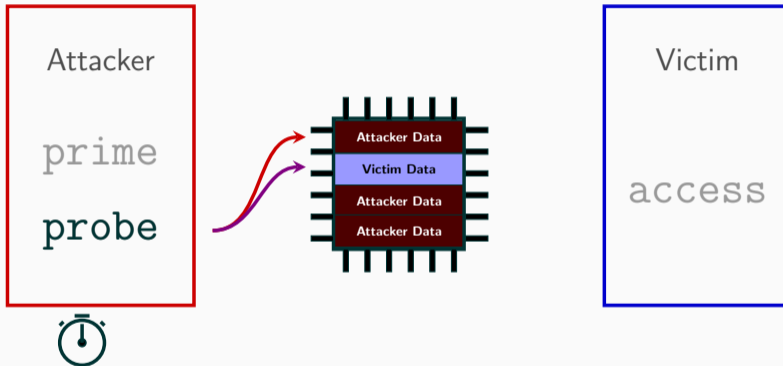


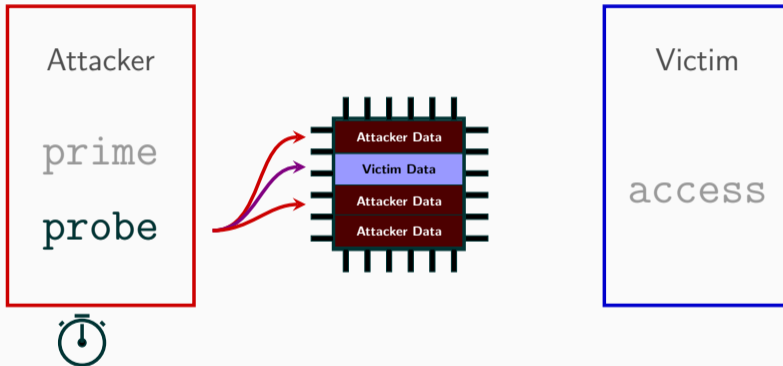


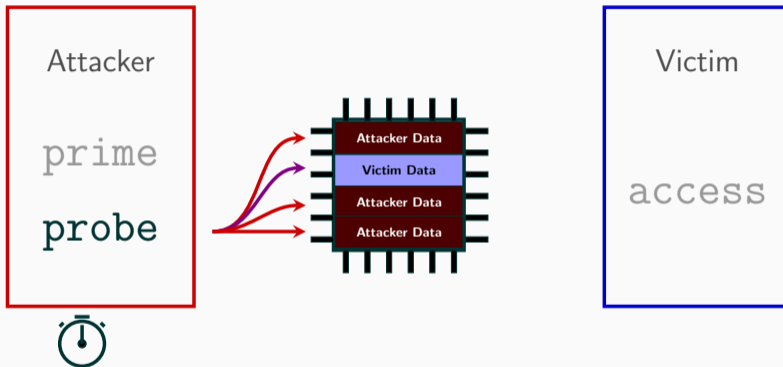


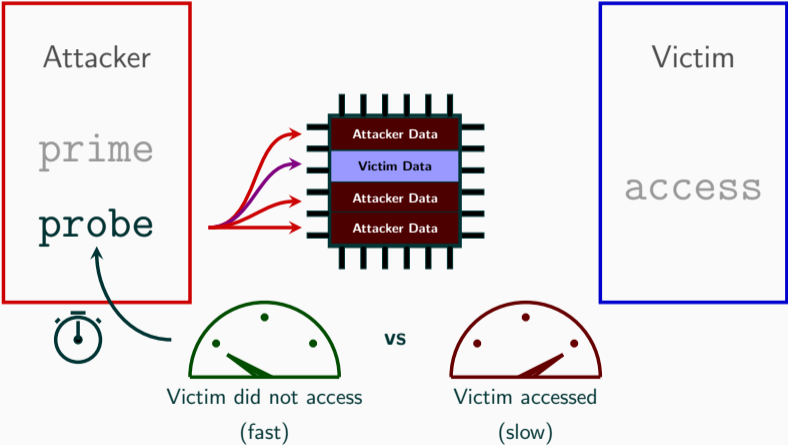


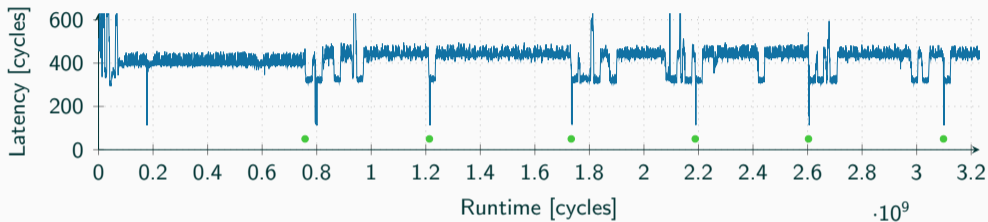




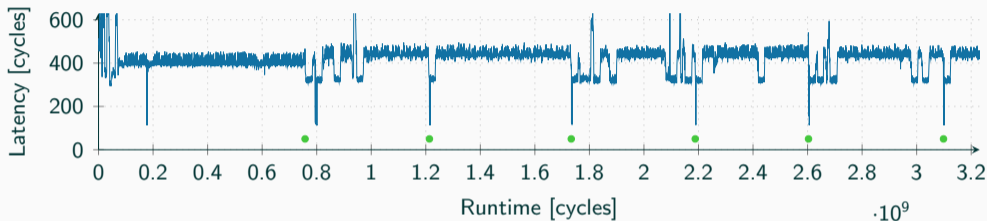




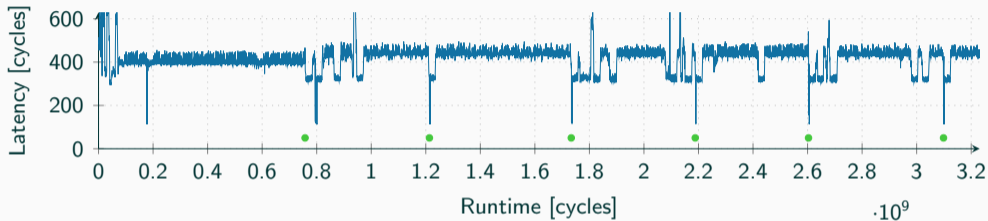




- Key presses trigger code execution in shared library (e.g., `libgdk`)

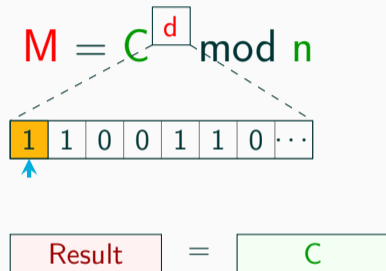



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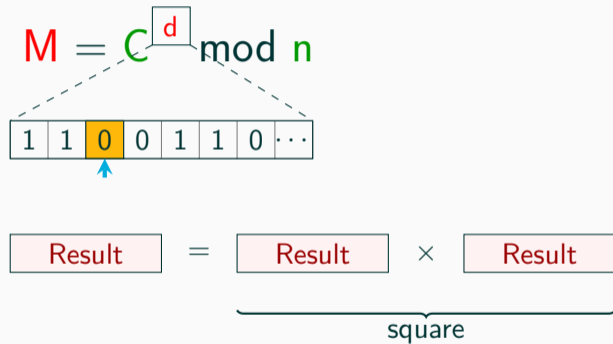
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- → Recover text with machine learning

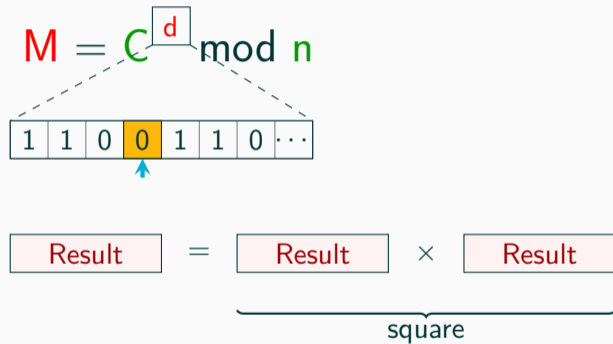
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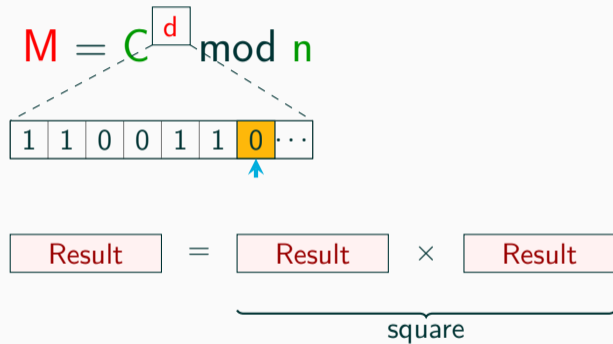
1 1 0 0 1 1 0 ...

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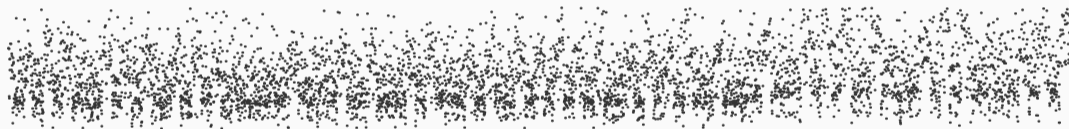
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1 | 1 | 0 | 0 | 1 | 1 | 0 | ...

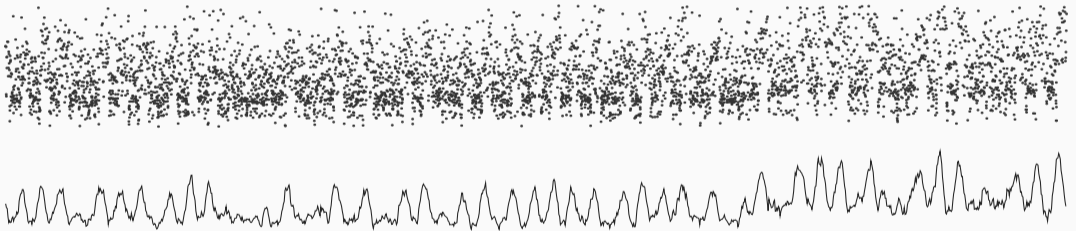
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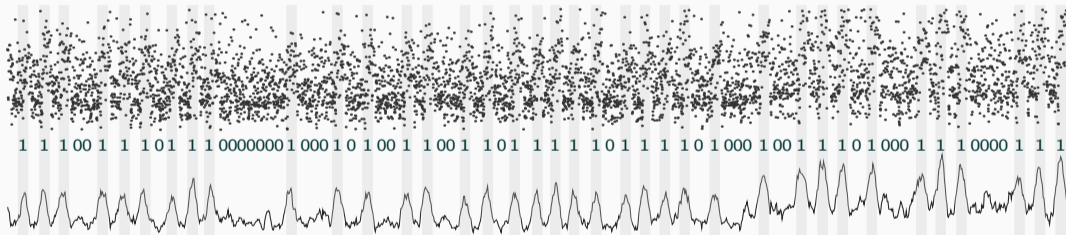
Raw Prime+Probe trace...



...processed with a simple moving average...



...allows to clearly see the bits of the exponent





- CPU vulnerability → out-of-order execution optimization



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- Similar to Meltdown



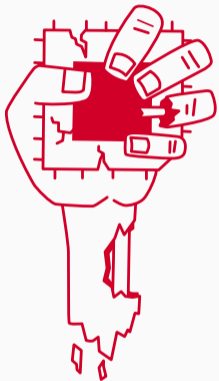
- Similar to Meltdown
- Forwarding non-present addresses to the L1 cache



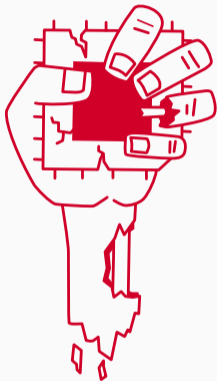
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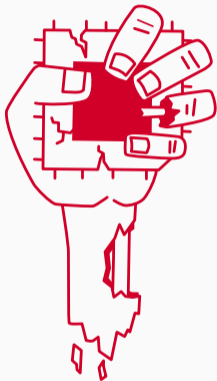
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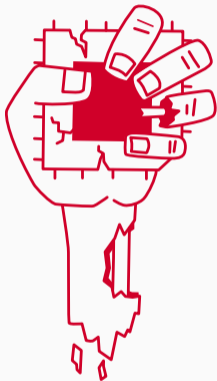
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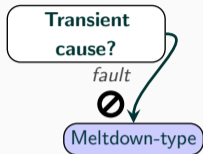


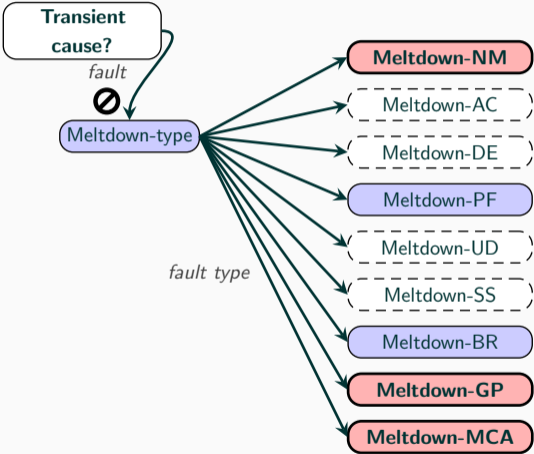
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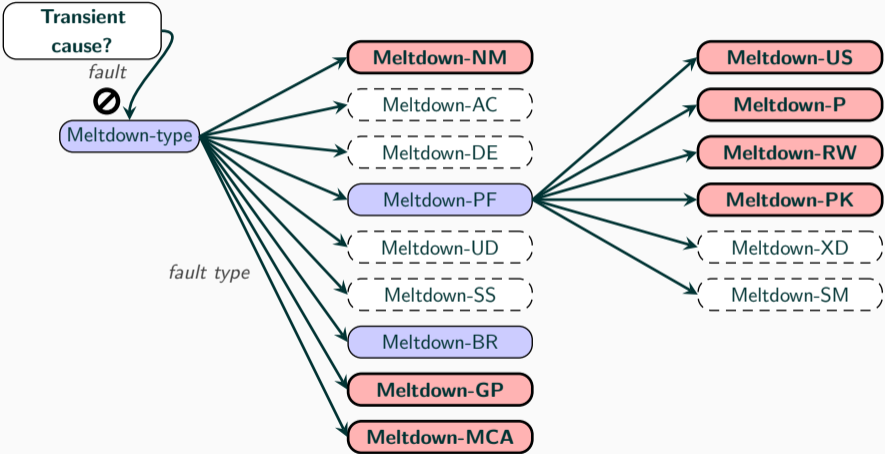


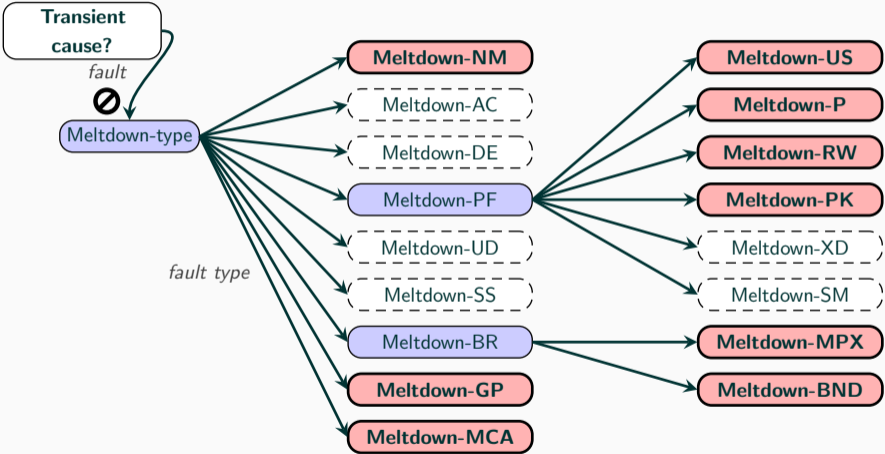
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**Transient
cause?**











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- Meltdown is **not** a fully **solved** issue
- The tree is extensible
- **More** Meltdown-type **issues** to come



- Mistrain CPUs internal predictors



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- CPU speculatively works with unintended values

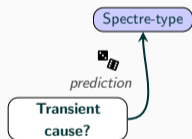


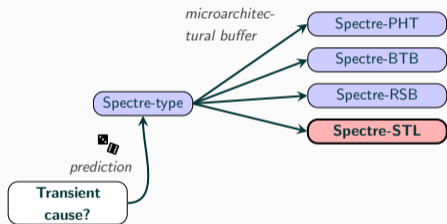
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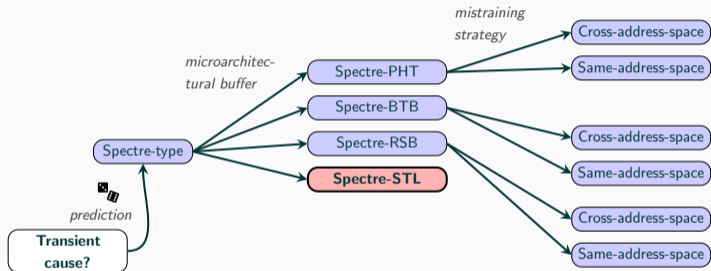


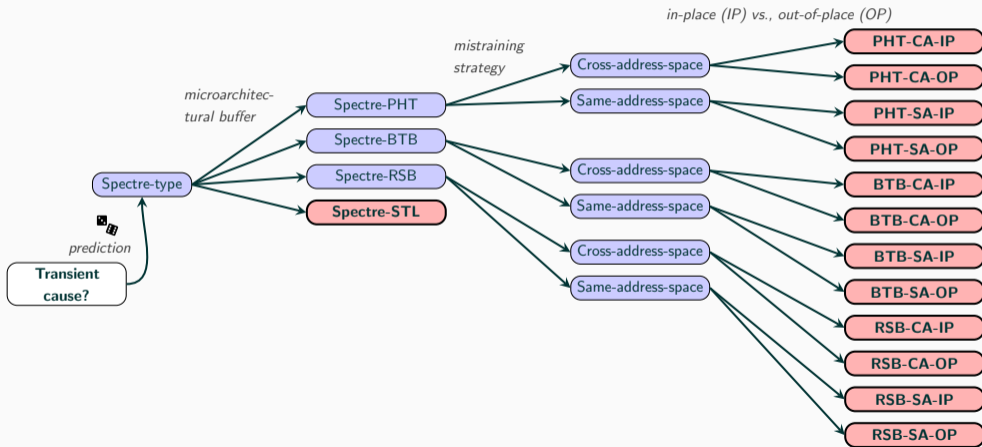
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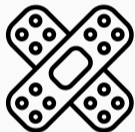
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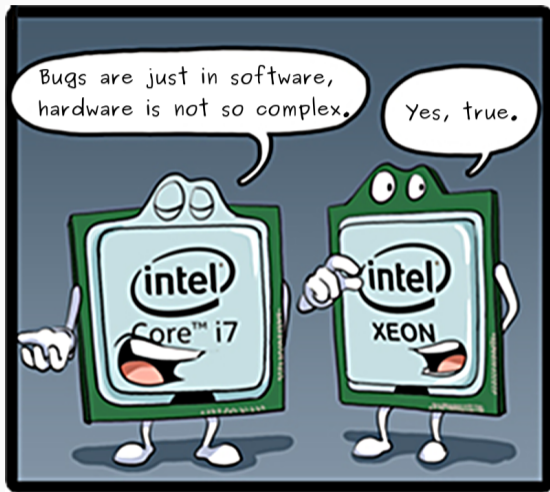
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- More isolation \rightarrow make exploitation harder
- Attacks on design difficult to fix
 - Caches \rightarrow we want timing differences
 - Prediction \rightarrow we don't want stalls
- So far: fixing symptoms



Original image from commitstrip.com

OS

CPU

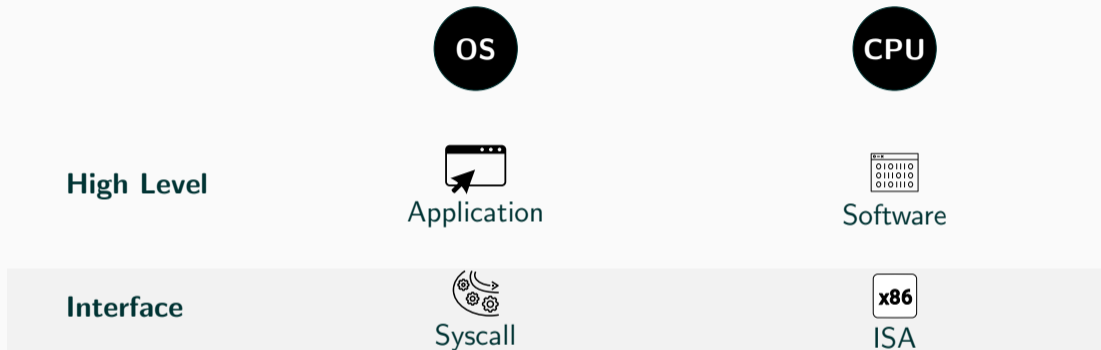
High Level

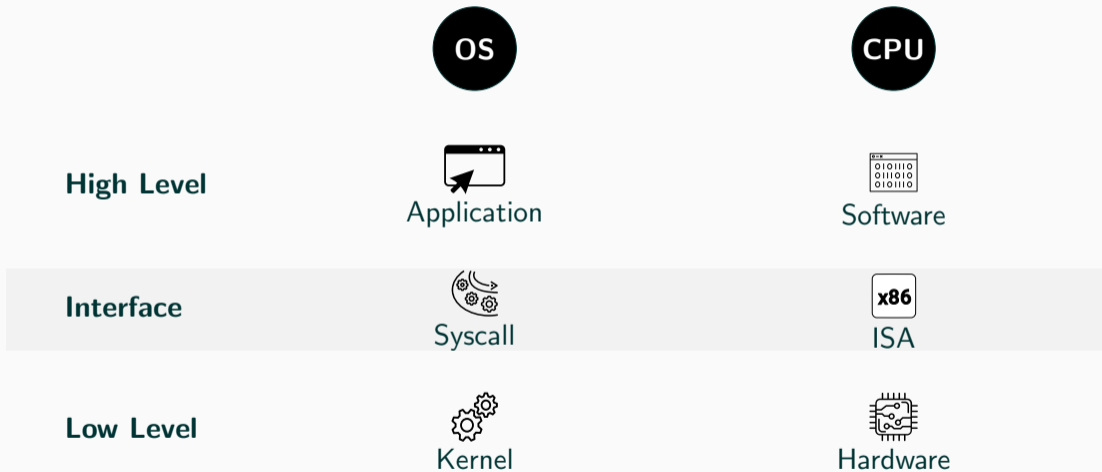


Application



Software





OS

CPU

OS

CPU

μ -arch. Interface



Non-standard Syscall

x86

ISA Extension

OS

CPU

μ-arch. Interface



Non-standard Syscall

x86

ISA Extension

μ-Architecture



Software Caches



Hardware Caches

OS

CPU

μ-arch. Interface



Non-standard Syscall

x86

ISA Extension

μ-Architecture



Software Caches



Hardware Caches



Software Prefetcher



Hardware Prefetcher

OS

CPU

μ-arch. Interface



Non-standard Syscall

x86

ISA Extension

μ-Architecture



Software Caches



Hardware Caches



Software Prefetcher



Hardware Prefetcher





- Managed by **operating system**



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- Buffers **file pages** in RAM for **faster accesses**



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- Ideally all file pages in page cache



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- Implemented by all major operating systems





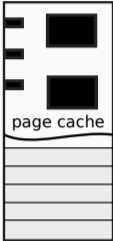
Victim

foo.so#1
foo.so#2
foo.so#3
foo.so#4

Address space



Disk



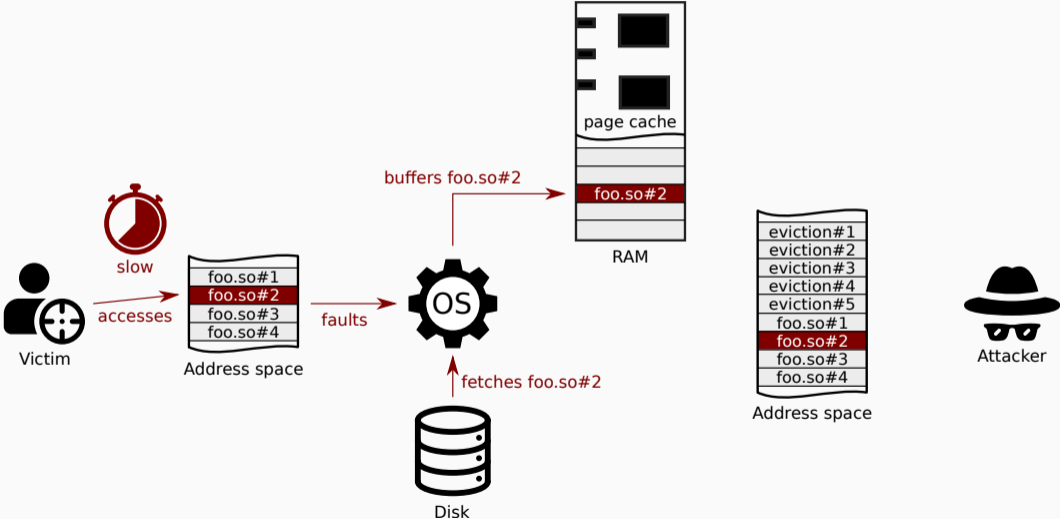
RAM

eviction#1
eviction#2
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eviction#5
foo.so#1
foo.so#2
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Address space

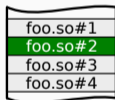


Attacker





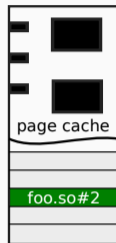
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Disk



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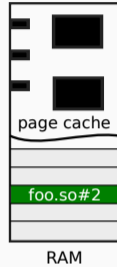
Attacker



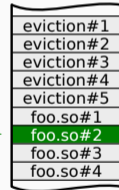
Address space



Disk



RAM



Address space



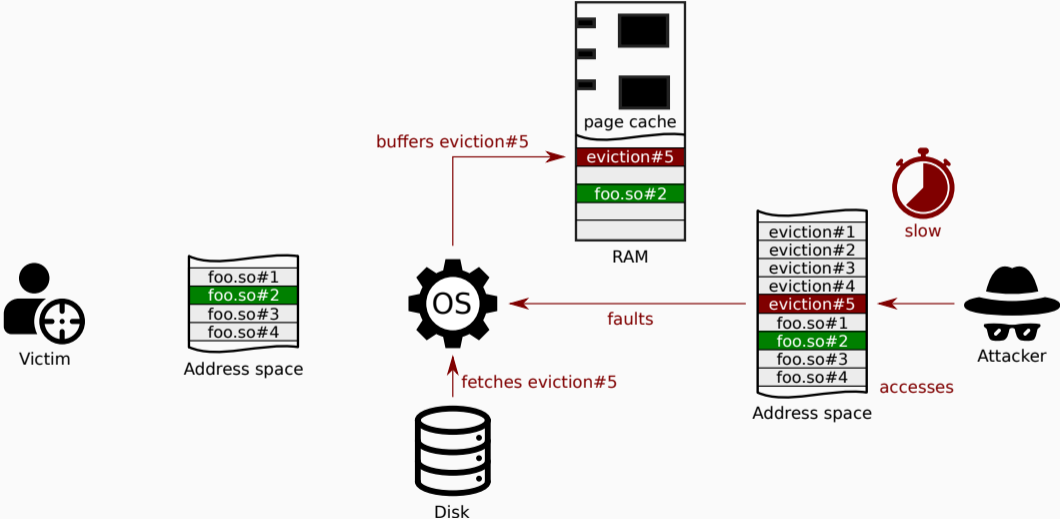
fast

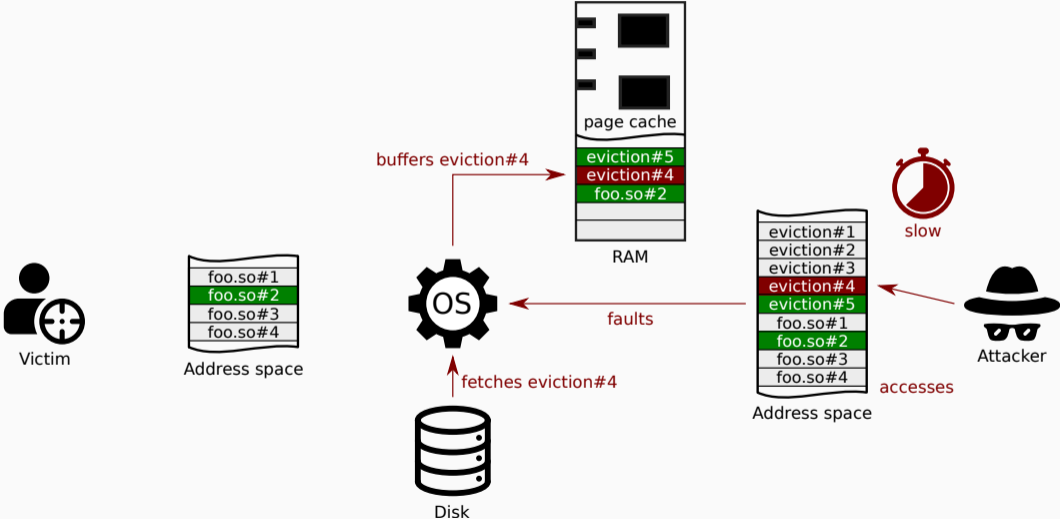
accesses

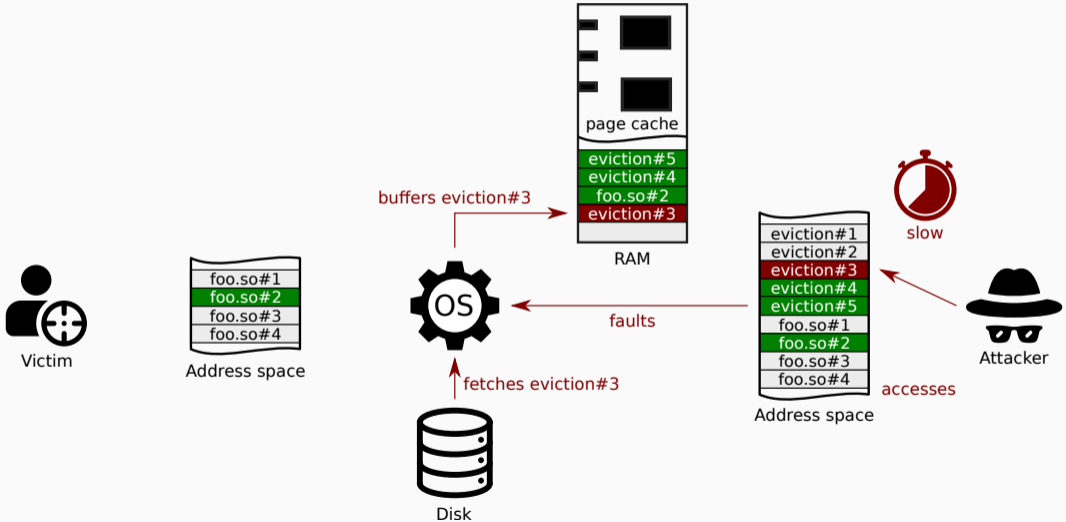


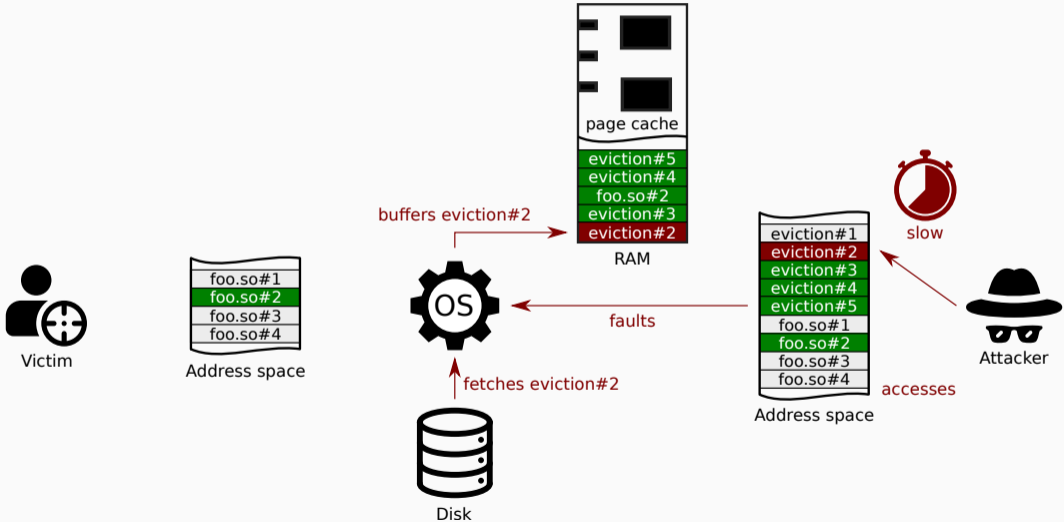
Attacker

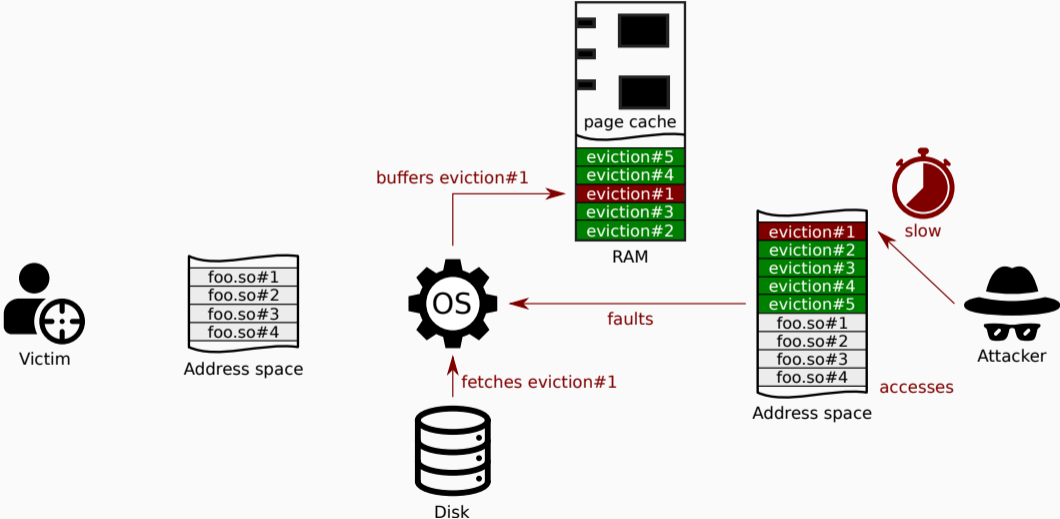














Victim

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foo.so#2
foo.so#3
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Address space



Disk



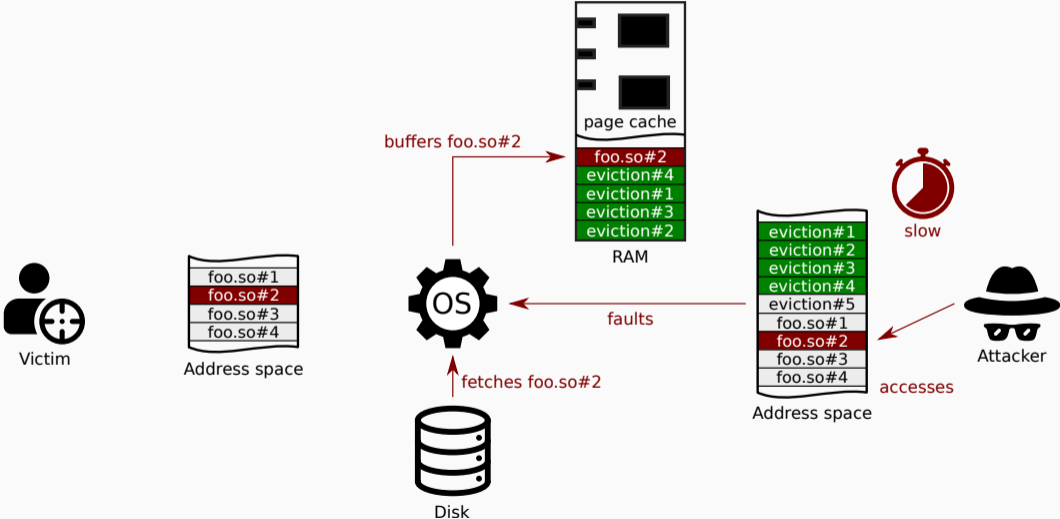
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mincore (2.04 μ s)





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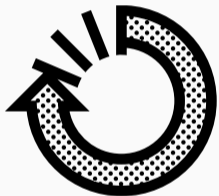
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- ... **presence** in working set
- ... **number** of working sets containing page (`ShareCount`)



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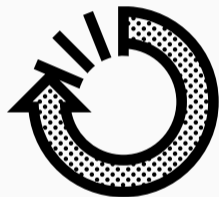
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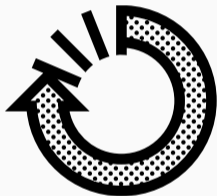




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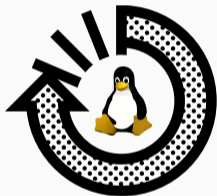
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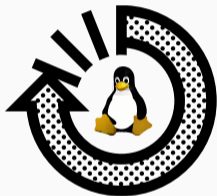




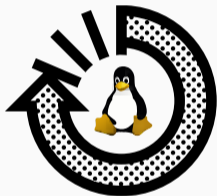
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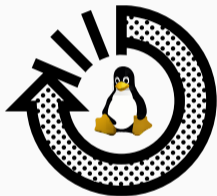




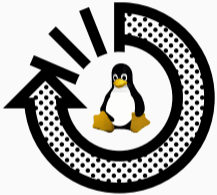
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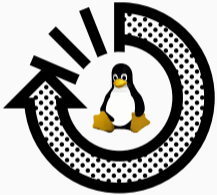
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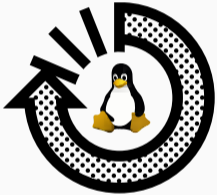
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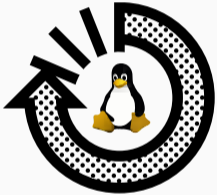
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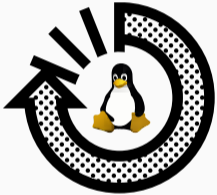
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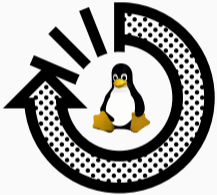
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- Average run time down to **149 ms** depending on optimisations

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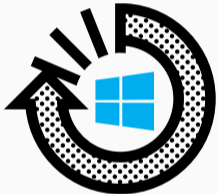
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Different implementation approaches:

OS	Eviction	Observation	Speed
Linux	like side channel	mincore	20.20 kB/s
	madvise	mincore	81.16 kB/s
	posix_fadvise		
Windows	process WS VirtualUnlock	QueryWorkingSetEx (ShareCount)	100.11 kB/s



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- **Low** bit error rate for all approaches (down to 0.000 03 %)

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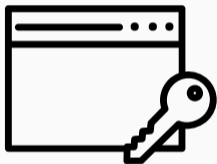


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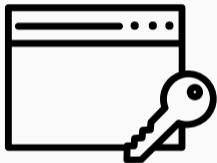


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- Average detection accuracy: **± 1 ms**

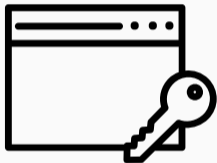




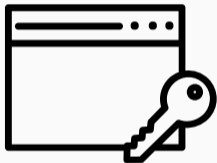
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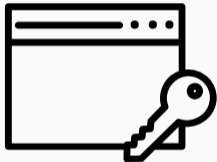
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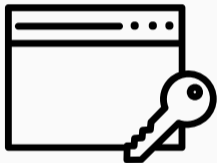
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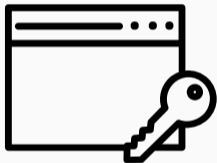
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 - Page-cache eviction already harder than on Linux



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 - Countermeasure currently under development



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- Every optimization is potentially a side channel



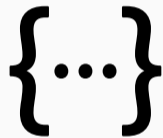
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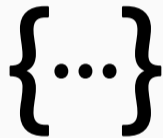
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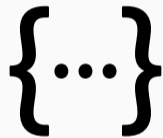
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- More optimizations → more side channels
- More attacks on the “OS microarchitecture”



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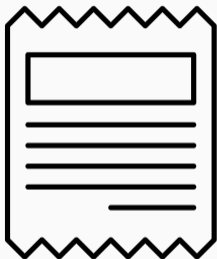


- **Abstraction** leads to side channels
- Software-cache attacks are similar to hardware-cache attacks
- Finding **countermeasures** is **difficult**

Are Microarchitectural Attacks still possible on Flawless Hardware?

Michael Schwarz

Erik Kraft



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